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Communication-less Protection Algorithms for Meshed VSC HVDC Cable Grids

Willem Leterme

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor of Engineering Science (PhD): Electrical Engineering

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Voorwoord

Hoewel een werk als dit typisch wordt beschouwd als geschreven voor een beperkt en gespecialiseerd publiek, wens ik met dit woordje elke lezer die dit proefschrift ter hand neemt, te gidsen doorheen het werk. Verder gebruik ik dit voorwoord graag om de mensen te bedanken die, rechtstreeks of onrechtstreeks, hebben bijgedragen bij het tot stand komen van dit proefschrift.

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Voor elk type lezer die dit werk wil bestuderen, bestaat er een optimale manier om het meeste inzicht uit dit werk te halen. De geïnteresseerde lezer met beperkte voorkennis kan een inleiding tot het onderwerp behandeld in dit proefschrift vinden in de eerste twee hoofdstukken, die de algemene en technologische context rond beveiliging van gelijkstroomnetten schetsen. De lezer met achtergrond binnen de energiesector kan tevens deze hoofdstukken gebruiken als springplank naar hoofdstukken 4 tot 7, die foutdetectie en de ontwikkelde beveiligingsalgoritmes uitdiepen. De lezer met een academische achtergrond vindt verdere theoretische uitwerking in hoofdstuk 3 en in de

appendices. De gehaaste lezer zal het eindpunt van dit werk, namelijk de conclusie, snel terugvinden.

Nu u als lezer weet hoe u dit proefschrift moet aanpakken, is het aan mij om een groot aantal mensen te bedanken.

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Il faut imaginer Sisyphe heureux. —
Albert Camus

Willem Leterme,
Oktober 2016

Abstract

For the large-scale integration of renewable energy sources into the power system, transmission corridors with power ratings and lengths greatly exceeding those in the existing power system will be needed. To realize these corridors, Voltage Source Converter High Voltage Direct Current (VSC HVDC) offers several advantages over the currently widely used ac technology. The use of VSC HVDC in a large-scale meshed grid can provide the major reinforcements to the power system needed for the integration of massive amounts of renewable energy sources.

Selective protection against dc side faults is essential to safely and reliably operate meshed HVDC grids. Since required operating times for HVDC grid protection are ten to hundred times faster than existing ac protection, HVDC grid protection algorithms are fundamentally different from those used in ac systems. Furthermore, the limited number of HVDC grid protection algorithms reported in the recent literature were only tested in specific small-scale test systems. For a generally applicable and reliable HVDC grid protection, a more fundamental approach towards the development of protection algorithms is needed.

This work provides the necessary concepts to develop communication-less protection algorithms for meshed HVDC grids. A detailed overview of dc fault phenomena is provided and fault clearing strategies proposed in the literature are discussed and classified. The fault current contribution of the half-bridge modular multilevel converter is characterized and a reduced converter model for dc fault studies, is proposed. Guidelines for the design of fault detection methods, based on fundamental traveling wave theory, are provided. Furthermore, signal processing requirements for protection algorithms, in particular required sampling frequency and digital filtering, are investigated. Finally, fast and selective HVDC grid protection algorithms for primary and backup protection are developed. These algorithms are tailored for selective fault clearing in VSC HVDC cable grids with inductive cable termination.

Samenvatting

Om hernieuwbare energiebronnen op een grote schaal te integreren in het elektriciteitssysteem, zullen corridors met vermogens en lengtes die vele malen groter zijn dan deze in het bestaande systeem, nodig zijn. Om zulke corridors te realiseren, biedt gelijkstroomtechnologie gebaseerd op Voltage Source Converters (VSC HVDC) verschillende voordelen ten opzichte van de hedendaags alomgebruikte wisselstroomtechnologie. Het gebruik van VSC HVDC in grootschalige vermaasde gelijkstroomnetten kan voorzien in de versterkingen die nodig zijn voor de integratie van massale hoeveelheden hernieuwbare energiebronnen.

Selectieve beveiliging tegen fouten aan de gelijkstroomzijde is essentieel voor de veilige en betrouwbare uitbating van vermaasde gelijkstroomnetten. Gezien de beveiliging van een gelijkstroomnet tien tot honderd keer sneller moet werken dan beveiliging van wisselstroomnet, zijn beveiligingsalgoritmes voor vermaasde gelijkstroomnetten fundamenteel verschillend van deze gebruikt in een wisselstroomnet. Daarenboven werd het kleine aantal beveiligingsalgoritmes beschreven in de recente literatuur enkel getest voor specifieke kleinschalige testsystemen. Om tot een algemeen bruikbare en betrouwbare beveiliging van gelijkstroomnetten te komen, is een meer fundamentele aanpak naar de ontwikkeling van beveiligingsalgoritmes noodzakelijk.

Dit werk voorziet in de concepten die nodig zijn voor het ontwikkelen van communicatieloze beveiligingsalgoritmes voor gelijkstroomnetbeveiliging. Een gedetailleerd overzicht van de fenomenen die optreden bij dc fouten wordt gegeven en de methodes om deze fouten te verwijderen, worden geclassificeerd. De bijdrage van HVDC convertoren, meer specifiek de “half-bridge modular multilevel converter”, tot dc foutstromen wordt gekarakteriseerd en een gereduceerd convertormodel voor gelijkstroomfoutstudies, wordt voorgesteld. Richtlijnen voor het ontwerp van foutdetectiemethodes worden voorgesteld op basis van fundamentele theorie van elektromagnetische golfpropagatie. Daarnaast worden voor deze methodes de vereisten naar signaalverwerking,

meerbepaald bemonsteringsfrequentie en digitale filters, onderzocht. Tot slot worden snelle en selectieve beveiligingsalgoritmes voor primaire en back-up beveiliging ontwikkeld. Deze algoritmes zijn afgestemd voor selectieve beveiliging van een gelijkstroomnet gebruik makende van kabels, waarbij de kabels afgesloten zijn met een inductieve impedantie.

Abbreviations

AAC	Alternate Arm Converter
ADC	Analog-to-digital Converter
CIGRÉ	Conseil International des Grands Réseaux Électriques
DEM	Detailed Equivalent Model
EC	Equivalent Circuit
EMT	Electromagnetic Transient
HIL	Hardware-in-the-loop
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
MI	Mass-Impregnated
MMC	Modular Multilevel Converter
OWF	Offshore Wind Farm
PWM	Pulse Width Modulation
SCR	Short Circuit Ratio
SOA	Safe Operating Area
TSO	Transmission System Operator
VSC	Voltage Source Converter

XLPE Cross-linked Polyethylene

List of Symbols

General

ϵ_{abs}	Absolute error
θ	Unit step function

Cable Modeling and Wave Propagation

Z'_{c}	Characteristic impedance of lossless line
F_1, F_2	Functions representing forward and backward traveling waves (frequency domain)
f_1, f_2	Functions representing forward and backward traveling waves (time domain)
ϵ_r	Relative permittivity
μ_r	Relative permeability
ρ	Resistivity
$\boldsymbol{H}$	Propagation matrix
$\boldsymbol{I}$	Current vector (frequency (phase) domain)
$\boldsymbol{I}_{\mathrm{m}}$	Current vector (frequency (modal) domain)
$\boldsymbol{T}_U, \boldsymbol{T}_I$	Modal transformation matrices
$\boldsymbol{U}$	Voltage vector (frequency (phase) domain)
$\boldsymbol{U}_{\mathrm{m}}$	Voltage vector (frequency (modal) domain)
$\boldsymbol{Y}_{\mathrm{c}}$	Characteristic admittance matrix
$\boldsymbol{Y}$	Admittance matrix

$\boldsymbol{Z}$	Impedance matrix
Γ	Reflection coefficient
τ	Propagation delay
H	Propagation function
T_I	Current refraction coefficient
T_U	Voltage refraction coefficient
v	Wave propagation speed
Y	Shunt admittance
Z	Series impedance
$Y_\mathrm{c}, Z_\mathrm{c}$	Characteristic admittance/impedance
γ	Propagation constant
A_1, A_2	Weight functions in weight function model
B_i, B_j	Voltage source for Thévenin equivalent cable model
I_{ji}, I_{ij}	Current source for Norton equivalent cable model

Converter Control and Modelling

C_arm	Arm capacitance
C^eq	Converter equivalent capacitance
C_SM	Submodule capacitance
$\hat{m}$	Modulation index
L_arm	Arm inductance
L^eq	Converter equivalent inductance
n_U,n_L	Upper/Lower arm insertion index
R_arm	Arm resistance
R^eq	Converter equivalent resistance
u_CU,u_CL	Upper/lower arm inserted voltage
u_CU^Σ,u_CL^Σ	Sum upper/lower arm capacitor voltage

i^{ref}	Current reference
$i^{\mathrm{u}}_{\mathrm{arm}}$,$i^{\mathrm{l}}_{\mathrm{arm}}$	Upper/Lower arm current
i_{leg}	Converter leg current
N	Number of submodules per arm
R^{off}	Power electronics off-state resistance (linear switch)
R^{on}	Power electronics on-state resistance (linear switch)
u^{Σ}	Sum capacitance voltage
$u^{\Sigma}_{\mathrm{leg}}$	Sum capacitor voltage in a converter leg
$u^{\mathrm{ref}}_{\mathrm{ac}}$	Leg reference ac voltage
$u_{\mathrm{c,i}}$	Submodule capacitor voltage
u_{SM}	Submodule output voltage

Fault Detection and Discrimination

$du^{\mathrm{thr}}, di^{\mathrm{thr}}$	Threshold on voltage/current derivative
R_{c}	Replica surge impedance
$u^{\mathrm{thr}}, i^{\mathrm{thr}}$	Threshold on voltage/current magnitude
$u_{\mathrm{r}}, i_{\mathrm{r}}$	Voltage/current at a relay
S_1, S_2	Directional detection function
u', i'	Superposed transient voltage/current
u^0, i^0	Pre-fault voltage/current
$u_{\mathrm{c}}, i_{\mathrm{c}}$	Voltage/current associated with cleared fault
$u_{\mathrm{uc}}, i_{\mathrm{uc}}$	Voltage/current associated with uncleared fault
y	Transformed voltage/current sample
y^{thr}	Threshold on transformed voltage/current sample
Δt_{BF}	Delay between breaker failure subsystem actions and primary relay detection instant
Δt_{pb}	Delay between backup and primary protection actions

Δt_{RF}	Delay between relay failure subsystem actions and primary relay detection instant
$\Delta t^{\mathrm{discr}}$	Time delay associated with fault discrimination
Δt^{d}	Time delay associated with fault detection
Δt^{int}	Time delay associated with fault current interruption
Δt^{o}	Time delay associated with breaker opening
t^{c}	Fault clearance instant
t^{d}	Fault detection instant
t^{f}	Fault inception instant
t^{o}	Breaker opening instant
t_{b}	Time instant associated with backup protection
t_{p}	Time instant associated with primary protection
t_{rb}	Time instant associated with remote backup protection

Signal Processing

ϵ_{pass}	Pass-band ripple
f_{c}	Cut-off frequency
f_{s}	Sampling frequency
$A_{\mathrm{pass}}, A_{\mathrm{stop}}$	Pass-band/Stop-band gain
B	Number of bits
h^l	Digital filter of length l
n	Filter order
T	Sampling time

System Parameters

$U_{\mathrm{ac}}^{\mathrm{prim}}$	Ac system voltage (grid side)
$U_{\mathrm{ac}}^{\mathrm{sec}}$	Ac system voltage (converter side)
L_{ac}	Ac system reactance

R_{ac}	Ac system resistance
S_{base}	Converter nominal rated power
U_{dc}	Dc voltage
U_{n}	Converter nominal voltage

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Chapter 1

Introduction

1.1 Research Context

The integration of massive amounts of renewable energy sources, such as the deployment of wind power plants or photovoltaics, to replace conventional power plants, such as coal-fired or nuclear power plants, results in larger and less predictable power flows in the power system. Compared with conventional power plants, renewable energy sources have a larger geographic spread. Furthermore, due to the dependency on weather conditions, generation from renewable energy sources, such as wind or solar energy, exhibits a variable power output with limited controllability. As a consequence, to replace generation using conventional energy source with these types of renewables, a larger installed capacity is needed, which results in larger power flows in the power system.

To deal with these large and volatile power flows, several studies identify the need for transmission corridors with power ratings and lengths greatly exceeding those of the existing power system. The grid development plan 2025 for Germany [1] foresees transmission corridors with a total length of 2600 to 3200 km and a capacity of 8 to 10 GW. The major part of these corridors must connect the wind power plants mainly installed in the northern part of the country to the load centers and photovoltaic power plants in the south. Within the European context, the development of renewable energy sources is identified as the main driver for transmission grid development in the ten-year network development plan by the European Network of Transmission System Operators (ENTSO-E) [2]. Also in this context, the grid development study for the European power system by 2050, e-Highway2050 [3], identifies the predominance of international

north-south corridors of several GWs for all scenarios under study. For scenarios with a large penetration of renewable energy sources, the study points out the grid development in the North Sea area necessary to harvest the high potential of offshore wind power in this region. For the United States power system, the study in [4] shows that by 2030, in the absence of electricity storage at a competitive cost, a higher interconnection of the currently loosely interconnected areas is a cost-effective way to deal with an increased penetration of wind and photovoltaic power plants.

Voltage Source Converter High Voltage Direct Current (VSC HVDC) systems are pointed out by the studies in [1, 3, 2] as a key technology for the realization of high power transmission corridors. Compared with ac technology, VSC HVDC offers the possibility to use long underground cables or long submarine connections, which enables the connection of remote offshore renewable energy resources. Furthermore, with VSC HVDC, active and reactive power can be independently controlled, thereby offering the possibility to support the stability of the connected ac system [5]. Over the past decade, several VSC HVDC point-to-point connections which connect offshore wind farms to the mainland and a number of links interconnecting asynchronous ac systems or links embedded in an ac system were commissioned [6]. In Europe, more VSC HVDC point-to-point connections are planned for the coming decade [2].

With multi-terminal VSC HVDC systems, efficiency can be increased and investment costs can be reduced compared with individual point-to-point connections if no additional dc fault clearing equipment is installed. Already in 2009, a multi-terminal VSC HVDC system was considered for the combined connection of offshore wind farms in the Baltic sea to the ac power systems in Germany, Denmark and Sweden [7]. Furthermore, between Sweden and Norway, a point-to-point connection was planned for commissioning in 2014, with an extension to a three-terminal system planned for 2019 [8]. However, these projects were discontinued since, in the first case, the Swedish transmission system operator (TSO) no longer supported the combined development [9]. In the second case, the extension to a multi-terminal system was canceled due to changes in market conditions and other grid investments in the Norwegian power system [10]. Nevertheless, in Europe, the interest in multi-terminal VSC HVDC systems has not faded as, e.g., a multi-terminal system is considered in the grid development plan of Germany [1] and studies are conducted for an offshore multi-terminal system between Ireland, Northern Ireland and Scotland [11] or an offshore hub in northeast Scotland [12]. Although in Europe, no multi-terminal VSC HVDC system yet exists, two multi-terminal VSC HVDC systems were recently installed in China. A three- and five-terminal system were commissioned in 2013 and 2014, respectively [13, 14].

Whereas point-to-point connections and multi-terminal systems are mainly used

to strengthen the existing ac system, the development of a meshed HVDC grid can provide a fundamental upgrade of the power system. The study in [15] showed that, compared with point-to-point connections, a meshed HVDC grid in the North Sea can decrease investment costs and increase cross-border interconnectivity in the countries surrounding the North Sea. To integrate renewable energy sources on a larger scale, visions for an overlay meshed VSC HVDC grid were proposed in the past, e.g., for Europe [16, 17] or Asia [18]. At present, the continued interest in meshed HVDC grids is reflected in (i) working groups of international organizations, e.g., CIGRÉ [19], (ii) initiatives from stakeholders, e.g., Friends of the Supergrid [20], and (iii) European funded projects tackling technical challenges for HVDC grids, e.g., Twenties [21], MEDOW [22], BEST PATHS [23] or PROMOtioN [24].

Despite technological advances and increased experience with VSC HVDC systems, several technical and non-technical challenges must be addressed to realize a meshed HVDC grid [25, 26]. These challenges are situated in the fields of control and protection, grid operation, modeling, grid planning and regulation.

1.2 Scope of the Work

This work focuses on protection of HVDC grids against dc short circuits (faults), and in particular on the design of selective communication-less protection algorithms for HVDC grids. Dc faults lead to abnormal operating conditions for which the HVDC grid is not designed. HVDC grid protection must remove these faults before these cause damage to components or lead to collapse of the system.

Dc fault clearing involves several steps: (i) fault detection, (ii) fault discrimination and (iii) fault current interruption. These steps are illustrated in Fig. 1.1 for an example four-terminal meshed HVDC grid, in which measurements, relays and breakers are located at each cable end. If a dc fault occurs on a cable, the dc voltage at the fault location attains a value close to zero. Due to the sudden change in voltage, electromagnetic waves are created at the fault location which quickly propagate throughout the grid. From the instant at which these waves have reached all terminals, fault current is fed by each of the HVDC converters (Fig. 1.1a). From the moment a wave pases a relay, it starts detecting the presence of a fault in the system, since the measured voltages and currents take values outside the normal operation area (Fig. 1.1b, in which each square indicates the detection of a fault). To selectively clear the fault by solely opening the breakers associated with the

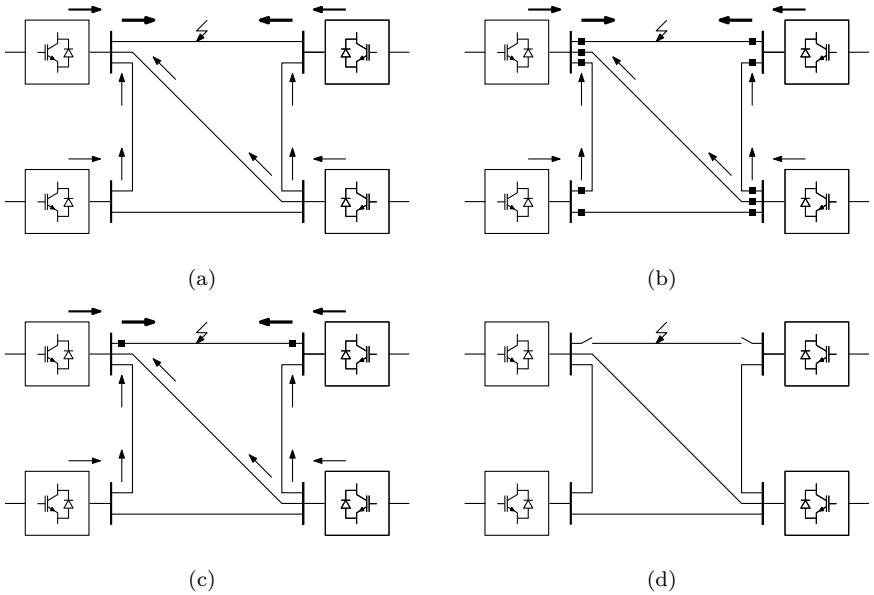


Figure 1.1: Consecutive steps in dc fault clearing: fault occurrence and current infeed by all terminals (a), fault detection (b), fault discrimination (c) and fault current interruption (d).

faulted cable, each relay needs to discriminate whether the fault is located on the cable with which it is associated or if it is located elsewhere (Fig. 1.1c, in which the squares indicate the identification of a fault on the associated cable). Finally, the relays associated with the faulted cable send a trip signal to their associated breakers to interrupt the fault current (Fig. 1.1d). In case this protection, i.e., the primary protection, fails, backup must be provided by the relays and breakers on the cables adjacent to the faulted cable.

The challenges for HVDC grid protection mainly arise from the short time available for fault clearing. In the most severe cases, dc fault currents rapidly reach high values whereas dc voltages quickly decrease. Since power electronic components can withstand only very limited overcurrents and only small deviations on the dc voltage are allowed for converter operation, HVDC grid protection must operate on a millisecond time scale, which is ten to hundred times faster than existing ac protection. Therefore, requirements on protection algorithms and fault clearing equipment for HVDC grids are fundamentally different from those currently used for ac protection.

The required high speed of operation poses challenges to the design of primary

protection algorithms for HVDC grids. HVDC grid primary protection algorithms, unlike those for ac grid protection, cannot make use of a fundamental frequency component and must operate during the transient stage in the fault current development. The transient voltages and currents measured at the relays are characterized by frequency-dependent phenomena such as wave propagation over cables and are influenced by the non-linear behavior of converters feeding in fault current. To accurately represent these phenomena, electromagnetic transient (EMT-) time domain simulations in EMT-type software are often performed using detailed models. However, these studies are not appropriate to design a primary protection algorithm which is generally applicable in a wide range of systems, since the complexity of such studies rapidly increases and conclusions mostly depend on the parameters used.

Furthermore, the required high speed of operation poses a challenge to the design of backup protection algorithms for HVDC grids. The design of backup protection algorithms, which are used in case of primary protection failure, faces a trade-off between speed of operation and reliability. Backup protection actions must be inherently delayed to not operate prior to the primary protection. Any additional delay enables the use of more secure algorithms on the one hand, but increases the total fault clearing time on the other hand.

1.3 Research Objectives

For this work, the main research objectives are (i) to develop a fundamental understanding of dc faults in HVDC grids and its associated modeling and (ii) to develop primary and fast backup protection algorithms for meshed HVDC grids.

Although several fast primary protection algorithms for HVDC grids were recently developed, e.g., in [27, 28, 29, 30, 31], a more fundamental approach to the design of selective HVDC grid protection algorithms is needed. In the literature, the recently developed protection algorithms were validated using EMT-simulations or real-time hardware-in-the-loop (HIL) tests for specific small-scale test systems. However, the applicability of the criteria used in these works often depends on the parameters used in these specific networks and general guidelines for the use of these methods are missing.

The backup algorithms proposed in the recent literature mainly adopt the philosophy as used in ac systems and consequently exhibit an unavoidable extensive delay between primary and backup protection actions. Backup algorithms to deal with breaker failure were proposed in [28] and [32]. Since these algorithms solely rely on current measurements, a delay is needed to allow

the primary protection to completely clear the fault before a failure can be detected.

The focus of this work is on protection of cable grids with half-bridge modular multilevel converters (MMCs). Cable grids are considered since these are the only possibility for offshore grids and public opposition against overhead lines drives policy makers more and more in the direction of underground cables, also for land connections. The converter topology studied in this work is the half-bridge MMC, as it is currently the converter topology provided by most major manufacturers. For dc breakers, series inductors are included as all presently proposed dc circuit breaker designs rely on a series inductor to limit the rate of current rise.

1.4 Structure and Contributions of the Work

The main contributions of this work are in Chapters 3-7 and can be classified in following domains: (i) dc fault current analysis, (ii) modeling for dc fault studies, (iii) fault detection, (iv) primary and (v) backup protection algorithms. The structure of the work and the main contributions per chapter are summarized in Fig. 1.2. Chapters 3 and 4 mainly relate to objective (i), i.e., fault current analysis, whereas Chapters 5 to 7 mainly relate to objective (ii), i.e. protection algorithm development.

Chapter 2 sets the framework for the research in this work by discussing HVDC technology from a protection perspective and providing a literature review on fault clearing strategies and protection algorithms for HVDC grids. The contributions of this chapter include a classification of fault clearing strategies with respect to HVDC grid protection objectives, fault clearing constraints and possible implementation in terms of fault clearing equipment.

Chapter 3 introduces the cable and converter models used for EMT-analysis of transients resulting from dc faults. To provide theoretical support for the remainder of the work, the mathematical representation of the cable is discussed as well as the approximations made for implementation of cable models in EMT-type software. The converter models implemented in EMT-type software used in this work are described and are used to analyze the contribution of the half-bridge MMC to dc faults. Based on this analysis, a reduced converter model for dc fault analysis is derived. The contributions in this chapter are (i) the analysis and characterization of the fault current contribution of the half-bridge MMC to dc faults and (ii) the development of a reduced equivalent circuit model for the half-bridge MMC, valid during all stages of the fault current development.

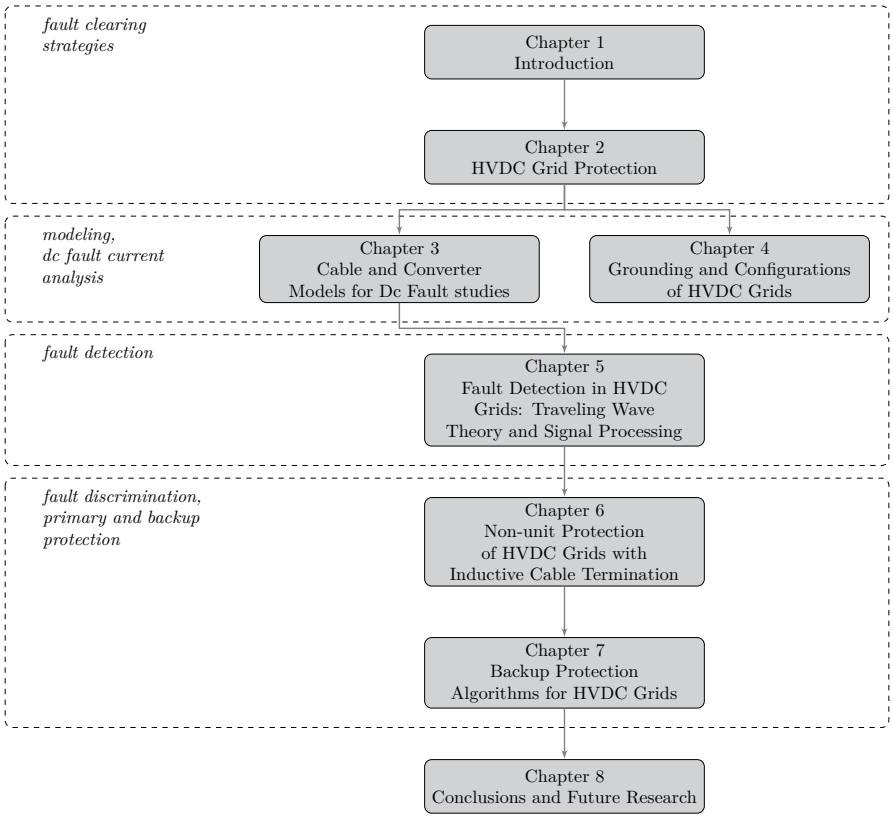


Figure 1.2: Structure of the work: flowchart of main chapters with keywords in italic.

In Chapter 4, an overview of grounding and configuration options for HVDC grids is provided. First, the options for grounding and configurations used in a point-to-point connection are described. Second, the impact of grounding and configurations on the transient and steaty-state fault currents and voltages are investigated through EMT-analysis. Third, the possible combinations of grounding and configuration options in a HVDC grid are discussed. The contributions in this chapter include (i) the identification of the main types of grounding and configurations for HVDC grids and (ii) an overview of the advantages and disadvantages of each grounding and configuration option in terms of dc fault handling, post-fault operation and grid extensibility.

Chapter 5 provides guidelines for the choice of fault detection signals in HVDC grids based on traveling wave theory and discusses requirements for measurement

equipment and digital filters. The approach is demonstrated with a case study on fault detection for a partially selective fault clearing strategy applied to a realistically dimensioned HVDC test grid. The main contributions in this chapter are (i) development of guidelines to determine the parameters and criteria for fast fault detection in HVDC grids based on frequency domain analysis, (ii) evaluation of the impact of the sampling frequency on the sensitivity and delay on fault detection and (iii) digital filter design for fault detection based on matched filter theory.

Chapter 6 deals with non-unit protection in HVDC grids by proposing a set of parameters which determine the protection zones along with an efficient method to analyze the thresholds on these parameters. The main contributions in this chapter are (i) the development of a protection algorithm for non-unit protection of a meshed HVDC cable grid with inductive cable termination and (ii) demonstration of the general applicability of this algorithm in HVDC cable grids with inductive termination, through a thorough sensitivity analysis for a wide range of grid and fault parameters.

In Chapter 7, fast backup protection algorithms are proposed to deal with breaker and relay failure. The main principles of these algorithms are first described, before testing in a four-terminal HVDC grid test system. The main contributions of this chapter are (i) development of principles for fast local and remote backup protection algorithms and (ii) development of methods to implement these principles.

Chapter 8 recapitulates the main conclusions and provides tracks for future research.

Appendices A-D support the main chapters by providing more detailed information on modeling, case parameters and mathematical derivations and providing additional simulation results.

Chapter 2

HVDC Grid Protection

HVDC grid protection differs from existing ac protection due to the differences in fault current characteristics and time scales. A HVDC grid, in which power electronic components have a limited overcurrent withstand capability and certain control time constants are in the millisecond time range, requires protection which is fundamentally faster than that of the existing ac system. Furthermore, dc fault currents have no natural zero crossings, which excludes the use of standard mechanical ac breaker technology.

This chapter provides an overview of HVDC grid protection in terms of technology, fault clearing strategies and selective protection algorithms for meshed HVDC grids. Section 2.1 discusses the state of the art in VSC HVDC converter, transmission line, dc circuit breaker and measurement technology. Thereafter, Section 2.2 presents fault clearing strategies for HVDC grids as proposed in the existing literature. Furthermore, these fault clearing strategies are classified based on the objectives of HVDC grid protection and fault clearing constraints. Protection algorithms used in ac systems and algorithms recently developed for HVDC grids are discussed in Section 2.3. Section 2.4 presents the conclusions of this chapter.

2.1 VSC HVDC Technology

This section discusses the state of the art in converter, transmission line, dc circuit breaker and measurement technology for VSC HVDC.

2.1.1 Converters

Since the installation of the first VSC HVDC system in Sweden in 1997 [33], several converter topologies have been in use [6]. The first generation converters was based on a two-level topology. With the second and third generation, the converter efficiency improved compared to the first generation. In this generation, a limited number of levels was added, leading to three-level converters. In the third generation, the two-level converter topology was again used, whereas converter controls were optimized to reduce losses. The converter topology currently provided by the major manufacturers, the modular multilevel converter (MMC), clearly differs from the first three generations in structure as in operation. Unlike the topologies from previous generations, these converters make use of a large number of voltage levels. The first converter of this generation was commercially installed in 2010 in the San Francisco Bay [34].

Essentially, the converter topologies of the first three generations show many similarities in structure and operation. These converter topologies, of which the two-level topology is shown in Fig. 2.1, consist of a capacitor at the dc side, a phase reactor at the ac side and six arms with a stack of insulated-gate bipolar transistors (IGBTs). For a two-level converter, the stack of IGBTs is essentially controlled as a single switch. By applying pulse width modulation (PWM), the converter's ac voltage is produced out of the dc voltage [35]. At the ac terminals of the converter, the resulting voltage waveform varies between u_{dc} and $-u_{\mathrm{dc}}$. The phase reactor L_{p} and additional ac filter (not shown in Fig. 2.1) are used to smooth the converter output to produce an ac voltage u_{ac} of acceptable quality. For multilevel converters, multiple voltage steps are used to generate an ac voltage, which reduces switching losses and filtering requirements. In practical applications, the number of levels was limited to three since further increase of the number of levels lead to problems with insulation of the converter valves [26].

Most major manufacturers have adopted the MMC topology as this topology has a higher efficiency and shows advantageous characteristics in its fault response compared with the previous generations [36, 37, 38]. In this topology, the converter arms consist of a series connection of a high number of submodules and an inductor L_{arm} (Fig. 2.2). These submodules consist of a capacitor and several switches, e.g., shown in Fig. 2.3a for a half-bridge submodule. The submodule capacitor carries a fraction of the dc voltage, equal to u_{dc}/N, in which N is the number of submodules per arm. By operating the switches, the voltage of the submodule capacitor can be inserted in the arm or bypassed. By varying the number of inserted submodules, the converter arm is used as a controllable voltage source to synthesize an ac waveform out of the dc voltage [39]. In some half-bridge submodule designs, a thyristor is used to protect the anti-parallel

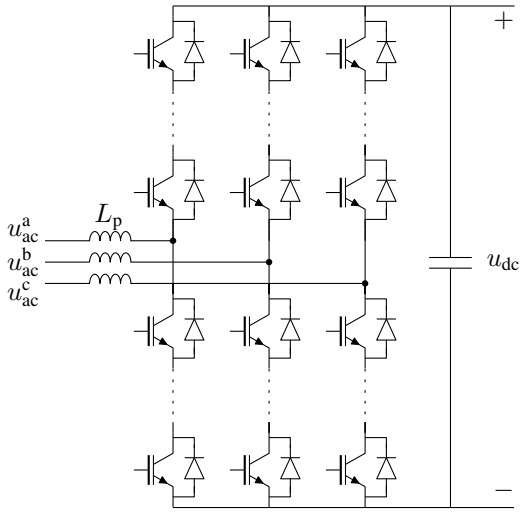


Figure 2.1: Two-level converter topology.

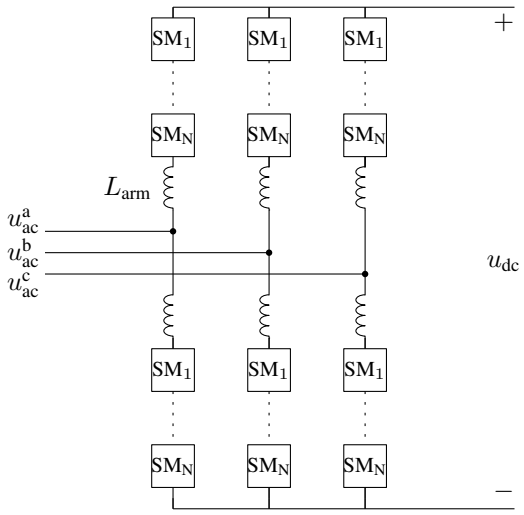
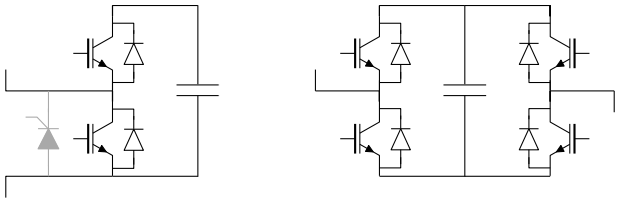


Figure 2.2: Modular multilevel converter topology.



(a) (b)

Figure 2.3: Half-bridge (a) and full-bridge (b) submodule topologies for modular multilevel converter.

diodes in case of faults (Fig. 2.3a). In Fig. 2.3a, additional equipment, such as a bypass switch connected between the submodule output terminals or a bleed resistor connected in parallel with the capacitor, is not shown.

For the first three generations, the response of the converter to dc faults can be treated in a similar fashion. In case of dc faults, the dc capacitor first discharges, before the converter feeds in fault current through the anti-parallel diodes [40, 41]. When the dc capacitor voltage falls below the ac voltage at the converter's terminals, the converter's anti-parallel diodes start conducting and the converter can no longer be controlled. Furthermore, the IGBTs are turned off to protect them against overcurrents. With all IGBTs turned off, the converter becomes an uncontrolled diode rectifier.

The response of the MMC to dc faults has favorable characteristics compared with the converters of previous generations [42]. MMCs do not use an external dc capacitor and the discharge rate of the submodule capacitors is limited since the arm reactors are in the fault current path. Second, the submodule capacitors can be stopped from discharging by turning off all IGBTs. Consequently, the rate of rise and initial peak of the dc fault current is lower compared with two-level topologies. After IGBT turn-off, the half-bridge MMC becomes an uncontrolled rectifier.

The MMCs can be categorized into converters without and with fault blocking capability. The half-bridge MMC is an example of a converter without fault blocking capability, since it becomes an uncontrolled rectifier if the IGBTs are turned off and consequently provides a path for ac fault currents. An MMC with full-bridge submodules (Fig. 2.3b) is an example of a converter with fault blocking capability. With full-bridge submodules, the submodule capacitor voltage can be used to oppose the ac voltage. Consequently, the dc current can be driven to zero and the converter blocks the fault current contribution of the ac system to the dc fault. As full-bridge submodules contain twice the number of

power electronic components of the half-bridge variant, the converter efficiency of a full-bridge MMC decreases compared with the half-bridge MMC [43].

Currently, research is conducted to develop alternative submodule or hybrid converter topologies which can block or limit the ac fault current while attaining an efficiency close to the one of the half-bridge MMC [44]. A hybrid topology, consisting of 50% half- and 50% full-bridge submodules per converter arm, has fault blocking capability and higher efficiency compared to the complete full-bridge MMC [45]. Second, various converter topologies can be designed by combination of a two-level topology and a series of submodules [46]. An example of this type of topologies is the alternate arm converter (AAC), in which the converter arms consist of a series connection of a stack of IGBTs with a number of full-bridge submodules [47]. Finally, several alternative submodule topologies have been proposed such as the clamped single- or double-cell submodule [48]. With these submodules, fault blocking can be achieved whereas the number of power electronics is decreased compared with the full-bridge submodule.

2.1.2 Transmission Lines

With the exception of one overhead line system [49], all currently installed VSC HVDC point-to-point connections make use of cables. In Germany, point-to-point connections making use of overhead lines are under consideration [1], although current policy prioritizes the use of underground cables [50]. For submarine applications, only cables can be used.

The main insulation materials used for HVDC cables are cross-linked polyethylene (XLPE) or mass-impregnated paper (MI) insulation. For VSC HVDC systems, XLPE is mainly used, since it offers several advantages over MI, such as higher power ratings per mass and an easier jointing process [51]. For existing VSC HVDC systems using cables, voltage ratings were limited to the voltage rating of the XLPE cable available at that time, with typical voltages of 80 kV, 150 kV or 320 kV [52].

Voltage ratings for XLPE are currently available in the range of 500 kV up to 525 kV [51, 53]. Nevertheless, the first VSC HVDC system employing a voltage of 500 kV makes use of MI cables [54]. Furthermore, a VSC HVDC point-to-point link with a voltage rating of 525 kV, currently in the planning phase, will also make use of MI cables [55].

2.1.3 Dc Circuit Breakers

To interrupt a dc fault current, dc circuit breakers are required to perform two extra functions compared to ac breakers; (i) drive the current to zero and (ii) dissipate the energy stored in the network after the fault. After fault current interruption, the breakers must withstand the resulting voltages in the system. With increasing voltage and current, the combination of these functions in a single device becomes increasingly complex. Consequently, in currently proposed dc circuit breaker topologies, these functions are separated over several parallel-connected devices [56].

In general, the parallel branches in a dc circuit breaker include a main conduction branch, one or more commutation branches and an energy absorption branch [56]. In normal operation, current only flows through the main conduction branch. To interrupt a dc fault current, the current in the main conduction branch is driven to zero with the aid of the commutation branches. Thereafter, the energy absorption branch dissipates the energy stored in the network and drives the current through the line to zero. The energy absorption branch typically consists of surge arresters which, beside absorbing the energy, protect the devices within the breaker against overvoltages.

The switch technology used determines the operation speed and maximum interruptible current of a dc circuit breaker. Dc circuit breakers can be categorized into power electronic breakers, hybrid breakers and mechanical breakers [57]. The former and latter breakers use power electronics or mechanical switches, respectively. Hybrid breakers use a combination of power electronics and mechanical switches.

Although power electronic breakers provide the shortest interruption times, the losses during normal operation make these breakers impracticable for HVDC. These type of breakers consist of a series of power electronics in the main conduction branch and a parallel surge arrester (Fig 2.4a). As the current is directly commutated from the main conduction branch to the energy absorption branch, no commutation branches are used in these types of breakers. Due to the large number of power electronics in the main conduction branch, these breakers exhibit high conduction losses during normal operation.

Mechanical breakers are slower compared with power electronic breakers but are capable of interrupting higher currents [58]. These breakers consist of a mechanical breaker in the main conduction branch, a resonant circuit in the commutation branch and a surge arrester (Fig 2.4b). The resonant circuit is an LC oscillatory circuit which is used to drive the current through the mechanical breaker to zero. In the passive resonant breaker, the resonance is triggered by the arc voltage when the mechanical breaker opens. The active resonant breaker

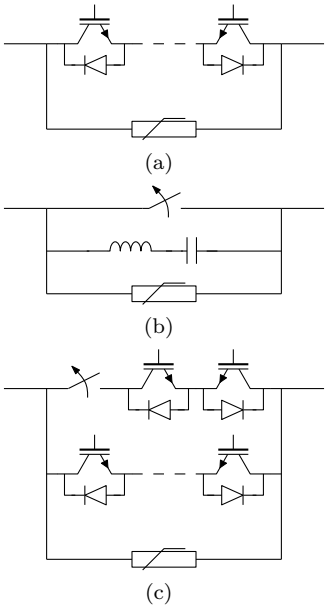


Figure 2.4: Examples of main breaker types: power electronic breaker (a), mechanical breaker (passive-resonant type) (b), hybrid HVDC breaker (c).

types use a precharged capacitor and a semiconductor switch or a spark gap in the commutation branch to trigger a forced oscillation. This increases the operation speed and maximum interruptible current compared to the passive resonant breaker.

By combining the advantages of power electronic and mechanical breakers, hybrid breakers achieve relatively fast operation times whereas losses in normal operation are limited. The main conduction branch consists of a series connection of a small number of power electronics and a mechanical switch (Fig. 2.4c). The power electronic switches first commutate the current to a commutation branch, after which the mechanical switch opens under zero current conditions. The commutation branch ensures that the voltage across the mechanical switch is limited until it can withstand the dc voltage. Finally, the commutation branch drives the current into the energy absorption branch, which drives the fault current in the line to zero. One recently proposed hybrid breaker topology makes use of a power electronic breaker in the commutation branch (Fig. 2.4c). With this topology, the current can be pro-actively commutated to the commutation branch, thereby avoiding the commutation delay to, e.g., provide fast back-up protection [59]. Other hybrid breaker topologies use capacitor snubber

circuits [38, 60] or full-bridge submodules in the commutation branch [14].

The currently existing prototypes of breakers can be classified according to their maximum interruptible current and interruption time. The prototypes of mechanical breakers proposed in [58] and [61] show a current interruption capability of 10 and 16 kA within 5 to 10 ms, respectively. The hybrid breaker prototypes discussed in [14, 59, 62] achieve an interruption capability of 5.5 to 15 kA within 2 to 3 ms. In [63], a mechanical switch for a hybrid breaker (also called ultra-fast disconnecting switch) which is able to withstand the main breaker switching voltage within 1.2 ms is reported.

All currently proposed breakers require a series inductor to limit the fault current rate of rise and to keep the current below the maximum interruptible current at the breaker opening instant. The series inductor decreases the rate of rise of the fault current during breaker opening. In [59], a value of 100 mH is proposed to limit the rate of rise of the fault current to 3.5 kA/ms in a dc system with a maximum voltage of 350 kV. To test the breaker proposed in [62], a test circuit generating a current with a rate of rise of 2.9 kA/ms was used.

2.1.4 Measurement Devices

Measurement devices are used to reduce the dc voltage and current to a low amplitude signal which is usable for the protection relays. These devices ideally have a linear response for a wide frequency range to accurately measure dc quantities as well as high frequency transients.

Typically, measurement devices for dc systems make use of a primary sensor (with optional primary electronics and a transmitting system) and a merging unit [64]. The primary sensor converts the high amplitude signal to a low amplitude one. In case electronics are used for the primary sensor, a transmitting system sends the sampled values to the merging unit. The merging unit converts the output of the primary sensor to a format usable for the relays.

This section discusses the technologies used for the primary sensors and transmitting systems, whereas the effects of sampling and filtering in the merging unit are discussed in Chapter 5.

Current Measurement

In HVDC systems, the primary current sensors which can be used are a zero-flux device, a hybrid electro-optical measurement or a fiber optic current sensor.

A zero-flux device uses magnetic cores around the conductor in which the flux flowing due to the current in the conductor is compensated to zero. Two main types of zero-flux devices exist. The first type, referred to as Direct Current Current Transformer (DCCT), consists of two cores with three windings, i.e., two windings to measure the flux due to the dc current and one winding to compensate this flux, as described in detail in [65]. The second type, referred to as Hall-effect current transformer, consists of a single core and winding and uses Hall-effect sensors to measure the flux. For both types, the current in the compensating winding is generated through an electronics circuit. This current is proportional to the current flowing through the conductor and is provided as output voltage through a high burden resistor. The bandwidth of these devices can be up to a few hundred kHz [66].

Hybrid electro-optical measurements combine an electrical sensor with optical transmission to provide isolation between the primary and secondary side of the measurement equipment. The measurements located at high voltage are converted into an optical signal which is transmitted to the low voltage secondary output of the measurement. An example of a hybrid optical current transducer used for dc systems is a combined shunt and Rogowski coil with optical transmission [64]. The shunt is used to measure currents close to dc, whereas the Rogowski coil is used to increase the bandwidth of the measurement device. The bandwidth of a Rogowski coil can be up to several MHz [67].

A fiber optic current sensor consists of a fiber optic cable wound around the conductor. This type of sensors make use of the Faraday effect, which relates the propagation speed of a polarized light wave to the magnetic field applied along the propagation direction. The two main types of these current transformers make use of polarized light waves which either propagate through the fiber optic in different directions around the conductor or propagate in the same direction with a different polarization [68, 69]. The difference in speed of these waves is a measure for the current through the conductor. Depending on the length of the fiber optic cables, the bandwidth of these sensors can be in the kHz to MHz range [70]. The output of these sensors is typically digital and transformed into different outputs (high/low power, analog, digital) using a merging unit [71].

Voltage Measurement

The main primary sensor used for dc voltage measurements is a capacitive compensated resistive voltage divider (RC-voltage divider), shown in Fig. 2.5. The basic building block of an RC-voltage divider is a parallel connection of a resistor and a capacitor. The series connection of a number of these parallel

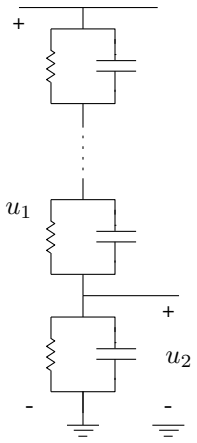


Figure 2.5: RC-voltage divider.

circuits enables to reduce the primary voltage u_1 to a smaller secondary voltage u_2 which can be provided to the measurements' electronic circuit.

With RC-voltage dividers, a high bandwidth in the order of a few MHz can be achieved [72]. In theory, the bandwidth of this device is unlimited, provided the RC-time constants of the primary and secondary part of the voltage divider are equal. In this case, the RC-voltage divider acts as a purely resistive divider for dc, whereas it acts as a capacitive divider for high frequencies. In practice, the bandwidth is limited due to resonance effects caused by stray inductances in the capacitive part [73].

Alternatively, an optical voltage transformer can be used. To measure the dc voltage, these optical voltage transformers make use of the Pockels effect, i.e., the induced birefringence in certain materials under application of an electric field [74]. These sensors make use of two orthogonally polarized waves, which are sent through an optical medium at which the voltage is applied. The phase shift between these polarized light waves after traveling through the material is a measure for the voltage.

2.2 Fault Clearing in HVDC Grids

The main task of HVDC grid protection is, besides guaranteeing human safety, to ensure power system security. Therefore, in case of faults, the protection should prevent damage to system equipment and avoid collapse of the power

system. To properly design HVDC grid protection, following specifications must be taken into account:

- Reliability: the protection must act in all fault situations and refrain from actions during normal operation. In the context of power system protection, the former characteristic is referred to as dependability whereas the latter refers to security.
- Selectivity and speed: the protection must isolate the faulted part of the system within a given time frame to avoid an unacceptable outage of the system.

The design of HVDC grid protection involves the selection of a protection philosophy and its practical implementation in terms of protection algorithms and fault clearing equipment. This design depends on a trade-off between several factors such as required system reliability, cost of components, cost of the protection system and frequency of occurrence and impact of the faults.

2.2.1 Dc Faults

Dc fault types

Dc faults can be roughly categorized into two types, i.e., pole-to-ground and pole-to-pole. Depending on the type of grounding, pole-to-ground faults either lead to high currents and low voltages or vice versa (cf. Chapter 4). Pole-to-pole faults result in high currents and low voltages irrespective of the type of grounding.

Faults can be permanent or temporary in nature. An example of a permanent fault is the failure of the cable insulation due to damage by ship anchors or insulation breakdown through ageing. An example of a temporary fault is insulator flashover due to a lightning strike on a conductor.

The major difference between cable and overhead line systems is the low probability of a pole-to-pole fault in the former system. Inherently, pole-to-pole faults on a cable system are connected via the ground. Furthermore, in cable systems, faults are typically permanent whereas in overhead line systems, permanent as well as temporary faults can occur.

Dc fault current development

The development of a dc fault current is characterized by different phenomena and events, as illustrated by Figs. 2.6 and 2.7, taken from [75]. Fig. 2.6 shows the positive pole current measured at the converter 1 side of L_{13} in the system described in Appendix A and shown in Fig. A.1. This current was obtained for a pole-to-pole fault in the middle of L_{13}, occurring at at $t = 10$ ms, and using a series reactor L_{dc} of 100 mH at the end of each link. Two cases were considered, i.e., the fault remains uncleared or the fault is cleared by dc circuit breakers at the ends of L_{13}.

In Fig. 2.6, the fault occurs at t_0 and creates electromagnetic waves which travel towards the line ends. These waves reach the terminals of the faulted line at t_1, and are partly reflected to the fault location and partly transmitted to the terminals not directly connected to the faulted line, which they reach at t_2. At t_1, due to arrival of the fault wave, the voltage at bus 1 quickly decreases. Consequently, the converter submodules of converter 1 discharge and contribute to the increasing fault current. To protect its IGBTs, the converter blocks at t_3 and the ac system to which the converter is connected feeds in fault current through the converter's anti-parallel diodes. The fault current increases until it is interrupted at t_6 by a dc circuit breaker which is opened at t_4. In case the fault current is not interrupted, the fault current continues to increase, causing all converters to be blocked at t_5. After t_5, the fault current is fed by the ac systems and evolves towards a steady-state.

2.2.2 Constraints on Fault Clearing

The fault clearing time of each fault clearing strategy must be matched to the time scales imposed by the HVDC grid and the connected ac system.

First, the limited overcurrent capability of power electronics puts a constraint on the time available for fault clearing. The constraints imposed by the power electronics can be situated at the HVDC converter or at the dc circuit breaker (if based on power electronics). IGBTs have a limited range of currents and voltages they can safely turn off, characterized by the Safe Operating Area (SOA) [76]. Typically, the maximum current that can be safely turned off is twice the continuous conducting current [36]. Diodes or thyristors can withstand higher currents for a longer amount of time compared with IGBTs. The overcurrent capability for these devices is typically specified by the limiting load integral i^2t [77]. With this value, the peak current for a non-repetitive pulse of a certain duration can be calculated, provided the pulse has a similar waveform as a half-sine.

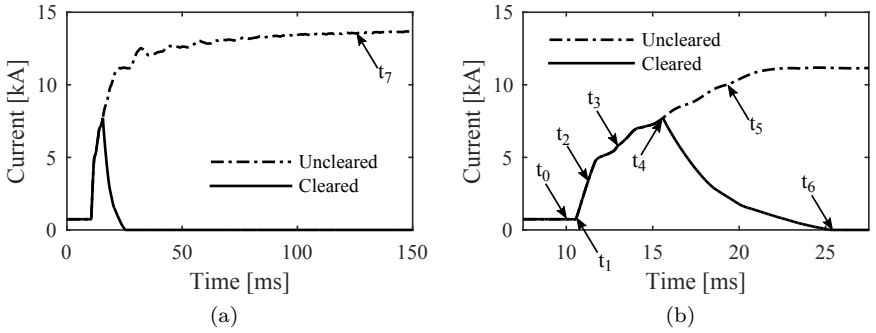


Figure 2.6: Fault current development in a HVDC grid.

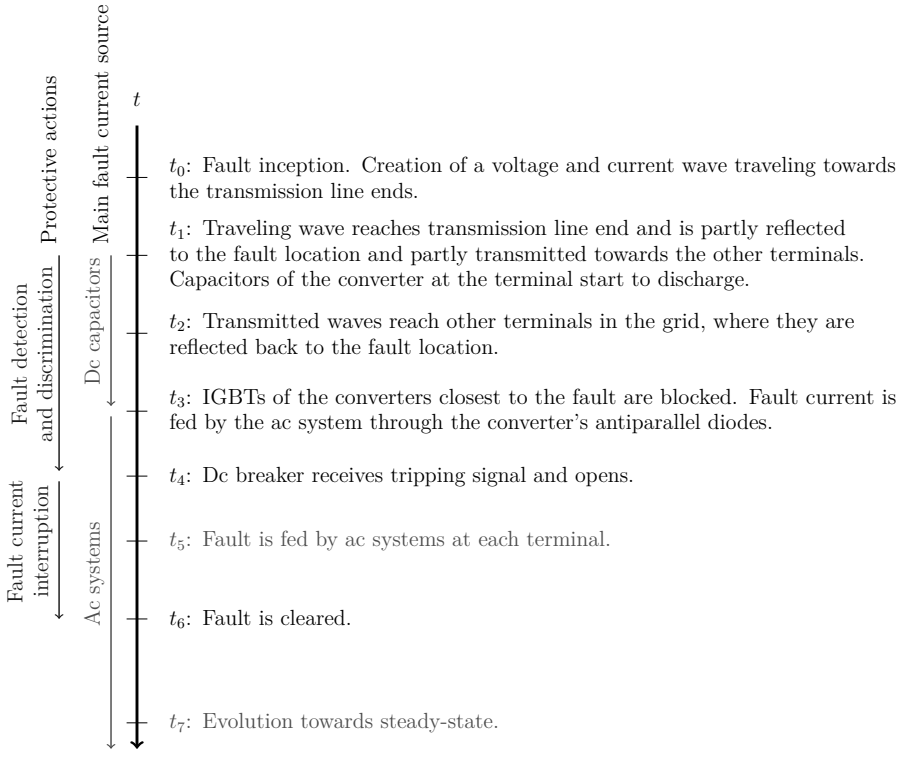


Figure 2.7: Sequence of events during a dc fault.

Table 2.1: Fault clearing strategies for HVDC grids.

(a)	Line
(b)	Line+
(c)	Open Grid
(d)	Grid-splitting
(e)	Low-speed HVDC grid protection

Second, the stability of the dc voltage in the HVDC grid forms a constraint on the speed of fault clearing. In the most severe case, a dc side fault causes, together with a fast increase of fault current, a fast decrease of the dc voltage. To avoid voltage collapse, the dc voltage must be kept within a narrow band around the nominal voltage [78].

Third, the impact of the disturbance resulting from a dc fault must be limited towards the connected ac system. The loss of power infeed should be limited to acceptable values for the ac system and the fault must be cleared in a timely manner to avoid loss of synchronism of the ac generators. For the latter constraint, the time scale is typically in the order of hundreds of milliseconds. Consequently, the constraints imposed by power electronics will probably pose more stringent constraints on fault clearing.

2.2.3 Fault Clearing Strategies for HVDC Grids

Several fault clearing strategies for HVDC grids, each aiming at different objectives, have been proposed in the literature. With each fault clearing strategy, a fault clearing time $t^{\mathrm{c}} - t^{\mathrm{f}}$ can be associated:

$$t^{\mathrm{c}} - t^{\mathrm{f}} = (\Delta t^{\mathrm{d}} + \Delta t^{\mathrm{discr}}) + (\Delta t^{\mathrm{o}} + \Delta t^{\mathrm{int}}), \tag{2.1}$$

in which t^{c} and t^{f} are the instants of fault clearance and inception, respectively. In (2.1), $(\Delta t^{\mathrm{d}} + \Delta t^{\mathrm{discr}})$ represent the time delays associated with fault detection and discrimination and $(\Delta t^{\mathrm{o}} + \Delta t^{\mathrm{int}})$ represents those with breaker opening and fault current interruption. By combining the appropriate protection algorithms with the interruption methods, the fault clearing time must be matched to meet the objective of the fault clearing strategy.

In published work by the author, i.e., in [79], five fault clearing strategies were identified and listed in Table 2.1. These strategies are classified in four main philosophies below.

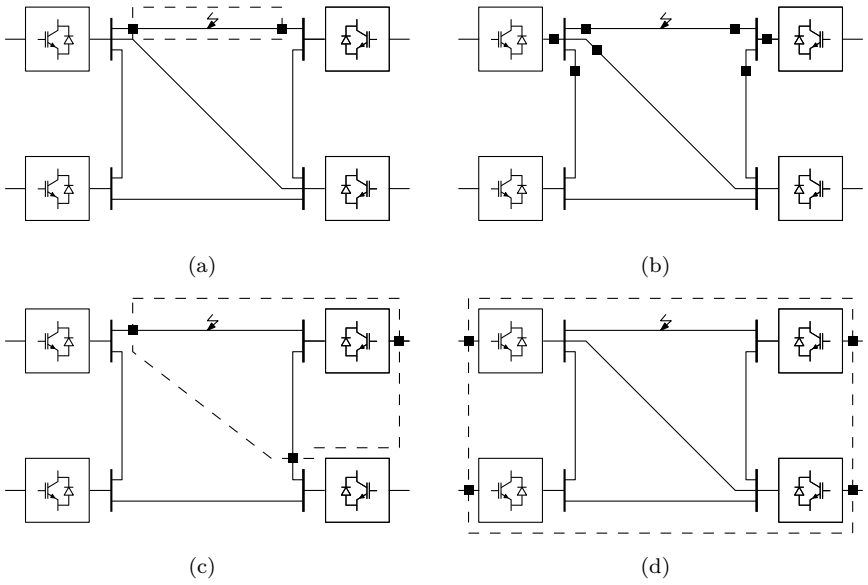


Figure 2.8: Fault clearing in example HVDC grid: selective (a), alternative (b), partially selective (c) and non-selective (d).

Selective Dc Side Fault Clearing

Selective HVDC grid fault clearing resembles ac system protection in the sense that each transmission line is individually protected. In case of a dc fault, only the faulted line is isolated, as illustrated in Fig. 2.8a.

Selective fault clearing can be done by using a selective protection algorithm in combination with dc circuit breakers at both line ends. The selective protection algorithm detects and discriminates faults, after which it trips the dc circuit breakers associated with the faulted line or cable. The combined fault clearing time should be small enough to avoid collapse of the dc voltage and to avoid damage to power electronic components. For certain breaker types, e.g., the one proposed in [59], the fault discrimination time Δt^{discr} can be excluded from the total fault clearing time, if $\Delta t^{\text{discr}} < \Delta t^{\text{o}}$.

The “line” and “line+”-strategies fall under the selective fault clearing strategies. The difference between both strategies is that in the former, no converters are allowed to block, whereas in the latter, the converters adjacent to the faulted line are allowed to block. Consequently, the “line+”-protection poses less stringent constraints on fault clearing times or equipment compared with the

"line"-protection.

These strategies require dc circuit breakers at the end of every transmission line. As an advantage, no constraints are imposed regarding the layout or size of the HVDC grid.

Alternative Dc Side Fault Clearing

An alternative approach to dc fault clearing or "Open Grid"-protection was introduced in [80].

In this approach, the time before fault current interruption is reduced by first non-selectively tripping breakers based on a local fault detection, before reclosing all breakers on the healthy lines. With this protection sequence, the breakers start interrupting after t^{d} instead of $t^{\mathrm{d}}+\Delta t^{\mathrm{discr}}$. Furthermore, the energy to be dissipated during fault clearing is shared over multiple breakers, thereby reducing the required energy absorption capability per breaker [81].

For this protection sequence, the protection algorithm or coordination of relays might be more difficult compared with selective dc protection, since protection zones cannot be clearly defined. First, non-selective tripping of breakers might lead to an unpredictable pattern of opening of breakers throughout the HVDC grid. Second, transients due to reclosing might interfere with identification of the faulted line. In work associated with this research, i.e., in [81], a strategy to implement this approach by only opening breakers at the bus adjacent to the faulted line was proposed, as shown in Fig. 2.8b.

Partially Selective Dc Side Fault Clearing

In a partially selective fault clearing or "grid-splitting" strategy, the HVDC grid is divided into protection zones which encompass multiple lines or converters [78]. These protection zones are divided by dc circuit breakers or equipment which can interrupt dc faults such as DC/DC-converters [82].

In case of a dc fault, the faulted zone should be swiftly isolated from the non-faulted ones to avoid voltage collapse in the latter [57, 83]. To clear the fault in the faulted zone, one of the options in the non-selective fault clearing strategy can be applied. Thereafter, the voltage in the faulted zone is restored and the zones must be reconnected.

Fig. 2.8c illustrates this strategy for a four-terminal HVDC grid, which is divided into two protection zones using dc circuit breakers at two locations. The fault

shown in Fig. 2.8c is cleared using the dc circuit breakers and the ac breakers of the converter in the faulted zone.

This strategy limits the need for dc circuit breakers, but imposes constraints to the layout and the size of the HVDC grid. First, the loss of the active power infeed or offtake by all converters within each dc protection zone must be limited to acceptable values for the underlying ac systems. Second, the power flow between the dc protection zones must be limited, since the loss of dc power infeed or offtake should not lead to unacceptable dc voltages in a non-faulted zone.

Non-selective Dc Side Fault Clearing

Within this strategy, the HVDC grid is considered as one protection zone and the entire HVDC grid is affected in case of dc faults. Since power flow in the entire grid must be restored after fault clearing, this strategy is also referred to as "low-speed HVDC grid protection".

In a first option, the entire HVDC grid is switched off in case of dc faults, as illustrated in Fig. 2.8d for fault clearing using the converter's ac breakers. After fault current interruption, the faulted line is isolated using disconnectors. Therefore, the faulted line needs to be identified either during fault current interruption or system restoration. Finally, the dc voltage in the non-faulted part of the HVDC grid is restored and power transfer is continued. Although the need for investments in dc side protective equipment is limited, the power system faces a temporary outage of the entire HVDC grid in case of dc faults.

To interrupt the fault current, the converter ac breakers, converters with fault blocking capability or dc circuit breakers at the converter terminals can be used [84]. The first method is similar to protection of currently installed point-to-point connections, which are protected against dc side faults by opening the ac breakers of both converters [49, 85]. By using the converters' ac breakers, the fault current interruption takes several cycles of the fundamental frequency (e.g. 40-60 ms) and converters are disconnected from the ac grid. The latter two implementations result in faster fault clearance and allow the HVDC converters to provide reactive power support to the underlying ac systems. A protection algorithm to detect the faulted line during system restoration was proposed in [86].

In a second option, the fault current infeed is limited at each of the converters. This enables the use of slower protection algorithms and breakers compared with the selective protection strategies. A low-speed protection strategy using fault current limiting at the converters is proposed in [87].

Summary

The fault clearing strategies proposed in the literature comply to different constraints and hence require different fault clearing equipment, as shown in Fig. 2.9. In Fig. 2.9, the letters indicating the strategy refer to those listed in Table 2.1.

If the objective of the HVDC grid protection is to protect the HVDC grid itself as a system, the constraints are mainly imposed by avoiding blocking of IGBTs or preventing dc voltage collapse and are in the order of a few milliseconds to a few tens of milliseconds. Consequently, for strategies (a), (b) and (c) and for the first part of strategy (d), i.e., isolating the faulty part of the HVDC grid, denoted by (d1) in Fig. 2.9, fast acting equipment is needed.

By contrast, if the objective of the HVDC grid protection is to minimize the effect of a dc fault on the ac system, constraints imposed at the dc side mainly arise from components such as diodes and thyristors whereas those at the ac side arise from the loss of power infeed. For these constraints, the time scales are larger compared with those for the previous strategies. Consequently, for the second part of strategy (d), denoted by (d2) in Fig. 2.9, and strategy (e), the speed of fault clearing equipment can be lower.

2.3 Protection Algorithms for HVDC Grids

The desired properties of a selective protection algorithm for meshed HVDC grids are, besides reliability, (i) high speed of operation, (ii) insensitivity towards variations in system conditions and (iii) simplicity. Any reduction in fault clearing time through fast algorithms can result in reduced breaker ratings or reduced series inductor sizes and can improve the stability of the HVDC grid. The insensitivity of the algorithm towards variations in system conditions results in a general application for a wide range of systems. Finally, methods relying on simple principles should be preferred whenever possible.

First, conventional and traveling-wave based protection algorithms for ac systems are introduced. Thereafter, the applicability of ac system protection for HVDC grid protection is discussed and the challenges for the design of HVDC grid protection algorithms are presented.

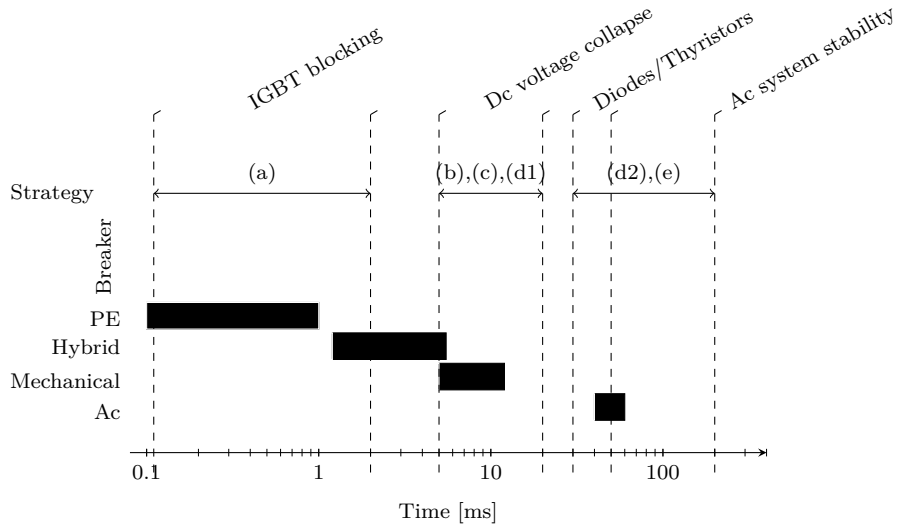


Figure 2.9: Overview of time scales for fault clearing constraints, strategies and equipment.

2.3.1 Types of Protection Algorithms

Protection algorithms can be categorized into algorithms making no use of communication (non-unit protection) and algorithms relying on communication (unit or non-unit pilot protection).

Non-unit protection makes use of measurements at a single location together with a relaying characteristic which defines the boundaries of the section of the grid it protects (the protection zone). The advantage of non-unit protection is its high speed due to absence of communication. The disadvantage is that the boundary of the protection zone is uncertain and depends on the quality of the measurements and the impedances in the system.

Unit protection compares the measurements at two locations in the grid to provide a closed protection zone.

Pilot protection uses information from the remote line end to provide a closed protection zone. Typically, pilot protection schemes based on non-unit protection can be divided into tripping and blocking schemes. In a tripping scheme, a relay is allowed to trip its associated breaker in the presence of a tripping signal received from the relay at the other end of the protection zone. In a blocking

scheme, a relay is allowed to trip its associated breaker in the absence of a blocking signal.

2.3.2 Ac System Protection

Conventional Protection Algorithms

In ac systems, overcurrent and distance protection are the two most common methods to provide non-unit protection. The coordination of overcurrent relays occurs through time or current grading. Overcurrent relays are typically used in radial systems, where the fault current is uni-directional, or as time delayed backup protection in meshed systems.

Distance relays calculate the impedance from the voltage and current measured at the relay location. In normal operation, the relay perceives an apparent impedance depending on the power flow over the transmission line. In case of a fault on the line, the calculated impedance is a measure for the distance of the fault on the line. Typically, the relay characteristic, defining the reach of the relay, is provided in the complex impedance plane. By comparing the calculated impedance to the relay characteristic, faults can be discriminated as within or outside of the protection zone. As distance relays are relatively insensitive to variations in source impedance, they are widely used in ac system protection [88].

To increase the speed of fault clearing, distance relays are employed in a pilot protection scheme. Distance relays can be coordinated using time grading of different zones or by using the relays at both ends of the line in a pilot protection scheme [89]. In a time grading scheme, the first zone is used for undelayed tripping of the breaker, whereas tripping for faults in the other zones is delayed to provide backup protection. The time intervals used in the grading scheme must account for delays on fault detection and fault clearing in the previous zones, and typically take values in the order of hundreds of milliseconds. Since the first zone does not cover the entire transmission line at which the relay is located, pilot protection schemes with distance relays are commonly used to increase the speed of protection for faults near the line ends.

Current differential protection is the main unit protection used in ac systems. For differential protection, fault detection relies on the difference between currents measured at both ends.

Traveling Wave-based Protection Algorithms

Traveling wave-based algorithms for ac system protection were proposed to increase the speed of protection compared with the conventional ac system protection. The speed of conventional algorithms is limited since information from a fundamental cycle (e.g., 20 ms in a 50 Hz system) is needed. Traveling wave-based algorithms make use of phenomena not related to this fundamental frequency and can hence increase speed of fault detection and discrimination.

Most traveling wave-based protection algorithms for ac systems make use of communication between the relays by either implementing a traveling wave differential algorithm or a directional comparison algorithm.

The traveling wave differential algorithm detects a fault by comparing the traveling waves calculated from measurements at both line ends [90, 91]. A detection criterion is made by subtracting the quantities measured at one end by a delayed version of the quantities measured at the other end. The delay must take into account the propagation delay of waves traveling over the line and the delay due to the communication channel. In case of a fault external to the line to be protected, the detection criterion takes values close to zero since the traveling wave entering the line is approximately equal to the traveling wave exiting the line. If a fault occurs between the line ends, the detection criterion detects a source of traveling waves between the line ends and takes a value proportional to the current through the fault.

With directional algorithms, the relays at both ends determine and compare the direction of the source of traveling waves. These algorithms trip the breakers if both relays detect a fault in the forward direction, i.e., a fault on the line protected by the relays. Different criteria were proposed to determine the source of traveling waves relative to the relay, e.g., the ones proposed in [92, 93, 94]. The tripping signals for the breakers associated with the relays can be determined by communicating the direction of the fault in a blocking or tripping scheme [91].

A number of communication-less traveling wave-based algorithms were analyzed in [91]. These algorithms determine the distance of the fault based on single-ended measurements. The distance of a fault on a line can, e.g., be estimated using the time between successive reflections of a traveling wave created by a fault [95].

Although these concepts can increase speed of protection compared with conventional ac system protection, they are not yet widely applied and did not yet replace the conventional ac system protection. Several reasons can be found in the literature, e.g.:

- some communication-less algorithms encounter difficulties in discriminating remote internal faults from close external faults [91],
- a high-speed and highly reliable communication channel is needed for the differential and directional algorithms. Furthermore, for the differential protection algorithm, precise time synchronization between the relays at remote ends is needed to avoid spikes in the detection function [91], and
- conventional capacitive voltage transformers cannot measure high frequency transients with a high fidelity [96].

2.3.3 Protection Algorithms for Meshed HVDC Grids

Clearly, conventional ac protection algorithms based on the fundamental frequency component are not applicable for HVDC grid protection. On the contrary, the detection criteria of traveling wave based ac system protection algorithms can be adapted for HVDC grid protection.

A variety of protection algorithms for non-unit protection of HVDC grids were proposed in recent literature. In [27], a set of fault detection criteria mainly based on current and voltage magnitude and derivative were used to design a selective protection algorithm. In this work, the capacitors of the two-level converters were used to define the boundaries of the protection zones. In [28, 29], the voltage derivative was used to discriminate faults. In [30], a protection algorithm using the Haar-wavelet on voltage and current measurements in combination with a voltage derivative-based criterion was used. The algorithm proposed in [31] uses a threshold on a detection signal which consists of a combination of voltage and current derivative to detect and discriminate faults in overhead line systems. In [28, 29, 30, 31], the breaker's series inductors are used to define the boundaries of the protection zones.

Although these algorithms rely on the same basic principles, a general approach to the design of non-unit protection algorithms for HVDC grids is still missing. The algorithms mentioned above were developed and validated using detailed EMT-simulations using small-scale test systems with specific grid and converter topologies and grid parameters. In [27, 28, 30, 31], the converter topology under study is a two-level converter. Within these test systems, in [27] and partly in [28], dc breaker series inductors are not considered, whereas in [30] and [31] these inductors are considered. In [29], half-bridge MMCs are considered together with dc breaker series inductors.

In [28] and [97], differential protection algorithms for meshed HVDC cable grids are proposed. The protection algorithm in [28] implements a differential

scheme based on currents. To compare the quantities at the remote ends, the measurements are compensated for communication delays, but not for traveling wave delays. Consequently, the algorithm needs to take into account a spike of short duration in the detection criterion in case of external faults. The algorithm described in [97] builds on the traveling wave differential algorithms originally developed for ac overhead line systems by including frequency dependency of cable parameters. This algorithm requires a precise characterization of the cable propagation function and characteristic impedance. Consequently, the application of the algorithm might encounter difficulties in case the protected link consists of many sections with different characteristics rather than a single section with homogeneous characteristics along its length.

2.4 Conclusion

Advances in VSC HVDC technology favor the development of a large-scale meshed HVDC grid. The current generation of converter topologies has a higher efficiency and lower peak fault currents compared with the topologies of the previous generations. The increase in cable voltage ratings allows to scale up power transfer. Current prototypes of dc circuit breakers demonstrate the ability to interrupt high currents within a few milliseconds, although they rely on series inductors to limit the current rate of rise. Finally, with current measurement technology, a wide bandwidth can be achieved, which enables capturing high frequency transients with a high fidelity.

In this chapter, an overview and classification of fault clearing strategies for HVDC grid protection is provided. The preferred fault clearing strategy depends on the objective of the HVDC grid protection. If the impact of a fault within the HVDC grid must be minimized, dc fault clearing is subject to stringent time constraints imposed by dc side phenomena and hence must make use of fast acting fault clearing equipment. If the focus of the HVDC grid protection is on minimizing the impact of a dc fault on the ac system, the time constraints on fault clearing are less stringent.

A large-scale meshed HVDC grid requires selective protection against dc side faults. Besides selective fault clearing, partially or non-selective HVDC grid fault clearing strategies are proposed. With these strategies, the ac system faces temporary outage of a large part of or even the entire HVDC grid in case of dc side faults. Such strategies fundamentally limit the size or structure of the HVDC grid, as dc sub-grids must be easily definable and the impact on the connected ac systems must be limited.

Fast protection algorithms are needed for selective HVDC grid protection. A small fault clearing time results in reduced required breaker ratings or reduced dc breaker series inductor sizes and can benefit the stability of the HVDC grid. Due to the required high speed of operation, algorithms for HVDC grid protection preferably rely on single-ended measurements in a non-unit protection scheme or make use of a fast communication scheme.

Currently, a general approach to the design of algorithms for HVDC grid protection is still missing. First, conventional ac protection algorithms cannot be straightforwardly applied since the response of the dc system to faults exhibits different characteristics compared with an ac system. Second, the algorithms for HVDC grid protection presented in the literature are developed based on extensive time domain simulations, although essentially, they make use of similar principles.

Chapter 3

Cable and Converter Models for Dc Fault Studies

The analysis of electromagnetic transients resulting from dc faults in HVDC grids requires an accurate representation of cables and converters. In this chapter, cable modeling for dc fault studies is reviewed in Section 3.1. Thereafter, converter modeling for dc fault studies is discussed in Section 3.2. Furthermore, in this section, the fault current contribution of the half-bridge MMC is analyzed and an equivalent circuit to represent the half-bridge MMC in dc fault studies is developed.

3.1 Modeling of HVDC Cables For Dc Fault Studies

The cable model should include the level of detail needed to accurately represent the waveforms associated with the type of study. Furthermore, the cable must be represented in a form which is suitable for the mathematical formulation associated with the type of analysis.

For time domain analysis of electromagnetic transients, two types of models can be used, i.e., lumped or distributed parameters [98]. The lumped (single-frequency) nominal pi-models can only be used to simulate short sections of cables for studies with a frequency range close to the one for which the parameters of the pi-model are evaluated. To accurately simulate long cables

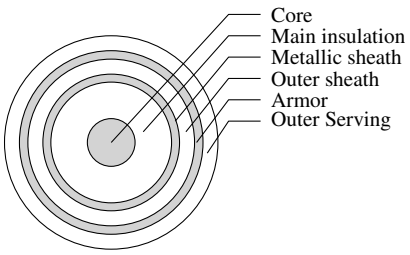


Figure 3.1: Underground cable design.

for dc fault studies, models which take into account the distributed nature and frequency dependency of the cable parameters are needed.

In Section 3.1.1, cable design for HVDC cables is discussed. Next, the mathematical representation of cables for analysis of power system transients is presented in Section 3.1.2. Thereafter, Section 3.1.3 reviews the distributed parameters cable models available in EMT-type software and describes the motivation for the choice for the model of [99] for the studies in this work. Finally, the cable models developed for the studies in this work are discussed in Section 3.1.4.

3.1.1 Cable Design

Underground cables consist of concentrically arranged conductors separated by insulation layers (Fig. 3.1). Land cables normally are made with two conductors, i.e., the core conductor and the metallic sheath. These are separated by a main and outer insulation layer (or outer sheath). The metallic sheath is used to prevent intrusion of water into the main insulation layer. The outer sheath protects the metallic sheath from corrosion and abrasion. Submarine cables have an extra conductor to increase the mechanical strength and an outer serving to protect the armor against corrosion and damages [100].

The main materials used for the core conductor are copper or aluminum. Materials used for the sheath conductor are copper, aluminum or lead. For the armor in submarine cables, steel is commonly used. The sheath is usually grounded at both ends and, in case of submarine cables, electrically connected to the armor at regular distances [100].

The materials primarily used for the main insulation layer of HVDC cables are XLPE or MI paper. For XLPE insulation, semiconducting layers are placed around the first insulation layer to reduce dielectric stresses in this layer [100].

The second insulation layer can be a polymeric sheath such as poly-ethylene (PE) or PVC. For submarine cables, the outer serving can be an extruded polymeric sheath or can make use of wound yarn layers. In the latter case, seawater is allowed to intrude into the armor [100].

3.1.2 Mathematical Representation

To represent a cable for EMT studies, several assumptions are made [101]. First, the cable conductors are assumed to be parallel and parallel to the earth surface. Second, the system is assumed to be homogeneous in the longitudinal direction. Third, transversal wave propagation is assumed.

Using the aforementioned assumptions, the cable can be described as a multiconductor system for which the line equations in the frequency (phase) domain are [101]:

$$\frac{d\boldsymbol{U}}{dx} = -\boldsymbol{Z}\boldsymbol{I}, \tag{3.1}$$

$$\frac{d\boldsymbol{I}}{dx} = -\boldsymbol{Y}\boldsymbol{U}, \tag{3.2}$$

in which $\boldsymbol{U}$ and $\boldsymbol{I}$ are the vectors representing the voltage on each conductor and the current through each conductor at distance x on the cable. The length of these vectors is equal to the number of conductors. The soil, in which the cable system is buried, provides the voltage reference and is an additional conductor.

The matrices $\boldsymbol{Z}$ and $\boldsymbol{Y}$ represent the per unit length series impedance and shunt admittance matrices for the cable. These are obtained from the cable system geometry and material properties, as discussed in greater detail in [98]. The series impedance $\boldsymbol{Z}$ depends on frequency due to skin effect in the conductors and the ground. The shunt admittance $\boldsymbol{Y}$ typically only consists of shunt capacitance and is frequency-independent.

In case the voltage on a conductor is assumed to be close to zero, the conductor can be mathematically eliminated using Kron reduction [102]. Through Kron reduction, the impedance and admittance of the eliminated conductor are combined with those of the conductor of the previous inner layer.

From (3.1) and (3.2), the wave propagation equations can be derived:

$$\frac{d^2\boldsymbol{U}}{dx^2} = (\boldsymbol{Z}\boldsymbol{Y})\boldsymbol{U}, \tag{3.3}$$

$$\frac{d^2\boldsymbol{I}}{dx^2} = (\boldsymbol{Y}\boldsymbol{Z})\boldsymbol{I}. \tag{3.4}$$

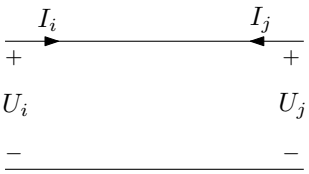


Figure 3.2: Cable voltage and current conventions.

After some manipulations, the solution of (3.3) for a line of length l can be formulated as, taking the conventions as shown in Fig. 3.2:

$$\boldsymbol{I_j} = \boldsymbol{Y}_\mathrm{c}\boldsymbol{U_j} - \boldsymbol{H}(\boldsymbol{I_i} + \boldsymbol{Y}_\mathrm{c}\boldsymbol{U_i}) \tag{3.5}$$

$$\boldsymbol{I_i} = \boldsymbol{Y}_\mathrm{c}\boldsymbol{U_i} - \boldsymbol{H}(\boldsymbol{I_j} + \boldsymbol{Y}_\mathrm{c}\boldsymbol{U_j}), \tag{3.6}$$

in which $\boldsymbol{Y}_\mathrm{c} = \sqrt{(\boldsymbol{YZ})^{-1}}\boldsymbol{Y}$ is the characteristic admittance matrix and $\boldsymbol{H} = e^{-\sqrt{\boldsymbol{YZ}}l}$ is the propagation matrix [103].

3.1.3 Cable Models for Time Domain Analysis in EMT-type Software

Several cable models exist for time domain analysis of electromagnetic transients. These cable models differ in the way they incorporate frequency dependency of the cable parameters as well as in the way they tackle the multiconductor arrangement. The cable models are first described for the single conductor case, after which the multiconductor case is discussed.

Single Conductor Models

For the single conductor case, a Norton or Thévenin equivalent circuit for the transmission line can be directly constructed based on (3.5) and (3.6) (Fig. 3.3) [104]. This equivalent circuit makes use of the propagation delay to decouple both ends of the cable. In Fig. 3.3, the characteristic impedance and propagation function are given by $Z_\mathrm{c} = \sqrt{Z/Y}$ and $H = e^{-\sqrt{YZ}l}$, respectively. The propagation constant $\gamma = \sqrt{YZ}$ consists of a real and imaginary part, which describe the attenuation and phase delay of a wave traveling from one

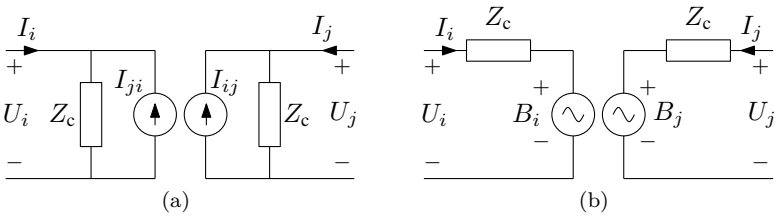


Figure 3.3: Norton (a) and Thévenin (b) equivalent circuit for frequency-dependent transmission line model.

end to the other. The voltage and current sources take following values:

$$I_{ji} = H(I_j + Y_c U_j) \tag{3.7}$$

$$I_{ij} = H(I_i + Y_c U_i) \tag{3.8}$$

$$B_i = H(U_j + Z_c I_j) \tag{3.9}$$

$$B_j = H(U_i + Z_c I_i). \tag{3.10}$$

In the context of traveling waves, the voltage sources $B_i = U_i - Z_c I_i$ and $B_j = U_j - Z_c I_j$ are related to the backward traveling waves at i and j, respectively. According to (3.9) and (3.10), these are related to the forward traveling waves at end j and i, $F_j = U_j + Z_c I_j$ and $F_i = U_i + Z_c I_i$, through the propagation function H.

Several options exist to derive an equivalent circuit suitable for time domain simulations in EMT-type software from the equivalent circuits of Fig. 3.3 [105]. These are the ideal line model, the lumped-resistance line (or Bergeron) model, a model using weight functions and the frequency-dependent parameters model.

The ideal line model assumes a lossless cable, i.e., the series resistance, skin effect in the conductors, influence of the ground resistance or losses in dielectrics are neglected [106]. Consequently, the characteristic impedance $Z_c^{id} = \sqrt{L/C}$ is real and constant* and the propagation function reduces to a time delay. In a time domain implementation, the current (or voltage) sources are dc sources for which the instantaneous current (or voltage) is equal to the forward traveling wave of the other line end delayed by the propagation delay $\tau = \sqrt{LC}l$.

The lumped-resistance line model or Bergeron model is a single frequency model which takes into account line losses by adding lumped resistances to the ideal line

*Since the series inductance is frequency-dependent, the constant value of Z_c^{id} depends on the frequency at which L is evaluated.

model [104]. The resistances are added to the ideal line model by dividing the line into two sections and adding one fourth of the line resistance at each section end. To increase attenuation for higher frequencies, the propagation characteristics can be split into low and high frequency paths, in an attempt to introduce some frequency dependency. The characteristic impedance and propagation delay, however, are evaluated at a single frequency. In ac system studies, e.g., relaying studies, this is typically the fundamental frequency. Choosing a frequency close to zero for dc fault studies results in a poor estimate of the propagation delay, as demonstrated in [107].

The model using weight functions introduces frequency dependency but assumes a constant characteristic impedance. In this model, the characteristic impedance is approximated by a real value $Z'_{\mathrm{c}} = \lim_{\omega\to\infty} Z_c$ and the voltages and currents at ends i and j are transformed into new variables B' and F':

$$B'_i = U_i - Z'_{\mathrm{c}} I_i, \tag{3.11}$$

$$B'_j = U_j - Z'_{\mathrm{c}} I_j, \tag{3.12}$$

$$F'_i = U_i + Z'_{\mathrm{c}} I_i, \tag{3.13}$$

$$F'_j = U_j + Z'_{\mathrm{c}} I_j. \tag{3.14}$$

After some manipulations, B'_i and B'_j can be described as a weighted function of F'_i and F'_j [108]:

$$B'_i = A_2 F'_i + A_1 F'_j, \tag{3.15}$$

$$B'_j = A_1 F'_i + A_2 F'_j, \tag{3.16}$$

in which the weight functions A_1 and A_2 depend on frequency and are given by

$$A_1 = \frac{1}{\cosh(\gamma l) + 1/2\,(Z'_{\mathrm{c}}/Z_{\mathrm{c}} + Z_{\mathrm{c}}/Z'_{\mathrm{c}})\sinh(\gamma l)} \text{ and} \tag{3.17}$$

$$A_2 = 1/2\,(Z_{\mathrm{c}}/Z'_{\mathrm{c}} - Z'_{\mathrm{c}}/Z_{\mathrm{c}})\sinh(\gamma l) A_1. \tag{3.18}$$

To avoid the use of A_2, the frequency-dependent distributed parameter models take into account frequency dependency of the characteristic impedance [109]. Consequently, $A_2 = 0$ and $A_1 = H$. The time domain implementation of the frequency-dependent cable model involves convolutions as H and Z_{c} vary with frequency [104]. To efficiently evaluate these convolutions in EMT-type software,

H is fitted in the frequency domain using rational functions [105]:

$$H \approx e^{-s\tau_\infty} \sum_{j=1}^{n} \frac{r_j}{s - p_j}, \tag{3.19}$$

in which r_j and p_j are the residues and poles of the fit which can be obtained by algorithms such as Vector Fitting [110]. The delay term $e^{-s\tau_\infty}$ is used to factor out the fast frequency variations in H and is, e.g., found by taking $\tau_\infty = \sqrt{C_\infty L_\infty} l$, in which $C_\infty = \lim_{\omega\to\infty} C$ and $L_\infty = \lim_{\omega\to\infty} L$ [111]. Additionally, dc correction techniques can be applied to improve the accuracy of the fit close to 0 Hz without extensively increasing the fitting order n [112]. Similarly, Z_c (or Y_c for the Norton equivalent model) is fitted in the frequency domain using rational functions.

Multiconductor Models

Due to mutual coupling of the conductors in a multiconductor system, a direct implementation of the circuits shown in Fig. 3.3 to a time domain equivalent circuit is not straightforward. In the literature, a multitude of approaches have been developed, which can be categorized into two main techniques: modal and phase domain techniques [98].

The modal domain techniques make use of eigenvalue analysis of $\boldsymbol{YZ}$ and $\boldsymbol{ZY}$ to transform the phase quantities of (3.1) and (3.2) to decoupled modal quantities. The modal transformation matrices $\boldsymbol{T}_I$ and $\boldsymbol{T}_U$ are obtained by:

$$\boldsymbol{\Lambda} = \boldsymbol{T}_I^{-1} \boldsymbol{YZ} \boldsymbol{T}_I, \tag{3.20}$$

$$\boldsymbol{\Lambda} = \boldsymbol{T}_U^{-1} \boldsymbol{ZY} \boldsymbol{T}_U, \tag{3.21}$$

in which $\boldsymbol{\Lambda}$ is a diagonal matrix. The voltages and currents in the modal domain, $\boldsymbol{U}_\mathrm{m}$ and $\boldsymbol{I}_\mathrm{m}$, are obtained by:

$$\boldsymbol{U}_\mathrm{m} = \boldsymbol{T}_U^{-1} \boldsymbol{U}, \tag{3.22}$$

$$\boldsymbol{I}_\mathrm{m} = \boldsymbol{T}_I^{-1} \boldsymbol{I}. \tag{3.23}$$

In the modal domain, each mode k can be solved independently as a single conductor. Finally, the modal quantities are again transformed to the phase domain using the inverse transformation of the one described in (3.23). The main challenge for this approach is to efficiently include the frequency dependency of $\boldsymbol{T}_I$ and $\boldsymbol{T}_U$. In some cases, e.g., in overhead line systems with a certain degree of symmetry, models using frequency-independent matrices to approximate

$\boldsymbol{T}_I$ and $\boldsymbol{T}_U$ provide accurate results [113]. However, in cases where frequency dependency of $\boldsymbol{T}_I$ and $\boldsymbol{T}_U$ cannot be neglected, e.g., in cable systems, a frequency domain fit for the transformation matrices must be used, e.g., as in the model proposed in [109].

The phase domain techniques directly solve (3.1) and (3.2). Several approaches exist to efficiently simulate cables in the phase domain in EMT-type software. Currently, the phase domain technique proposed in [99] is implemented in most existing EMT-type software [102]. This method makes use of a fit of the propagation matrix $\boldsymbol{H}$ and the characteristic admittance matrix $\boldsymbol{Y}_\mathrm{c}$. The fitting of $\boldsymbol{H}$ is done through following routine, as discussed in detail in [99, 111]:

1. Obtain a nearly diagonal matrix $\bar{\boldsymbol{\Lambda}} = \boldsymbol{T}_\infty^{-1}\boldsymbol{Y}\boldsymbol{Z}\boldsymbol{T}_\infty$, where $\boldsymbol{T}_\infty$ is a constant approximation for the frequency-dependent modal transformation matrix $\boldsymbol{T}_I$. Discard the off-diagonal elements in $\bar{\boldsymbol{\Lambda}}$ to obtain $\hat{\boldsymbol{\Lambda}}$.
2. For each diagonal element in $\hat{\boldsymbol{\Lambda}}$, extract a delay $\tau_{\infty,k}$ and calculate a frequency domain fit for each diagonal element in $\hat{\boldsymbol{H}}_\infty = e^{-\sqrt{\hat{\boldsymbol{\Lambda}}}l}$ as in (3.19).
3. Discard the residues of each fit and approximate the (phase domain) propagation function $\boldsymbol{H}$ as:

$$\boldsymbol{H} \approx \sum_{k=1}^{q} \left(\sum_{j=1}^{n_k} \frac{\boldsymbol{R}_{k,j}}{s - p_{k,j}} \right) e^{-s\tau_{\infty,k}}, \tag{3.24}$$

   in which n_k is the order of the fit for each diagonal element k in $\hat{\boldsymbol{H}}_\infty$ and q is the number of diagonal elements in $\hat{\boldsymbol{H}}_\infty$. To find the residues $\boldsymbol{R}_{k,j}$, a least squares fit is used.

Summary

The most accurate multiconductor cable models take into account frequency dependency of the propagation matrix and characteristic impedance. Whereas the model in [109] can, in some cases, encounter difficulties in finding a stable fit for the frequency-dependent transformation matrices, the model proposed in [99] is generally applicable. Since the model described in [99] is also adopted by most commercial EMT-type software, e.g., [114], this modeling approach is used in this work.

Table 3.1: Cable 1 geometry and material parameters.

	Outer radius [mm]	ρ [Ωm]	ϵ_r [-]	μ_r [-]
Copper Core	21.1	$1.68 \cdot 10^{-8}$	1	1
XLPE Insulation	37		2.4	1
Copper Screen	39	$1.68 \cdot 10^{-8}$	1	1
PE Insulation	48		2.3	1

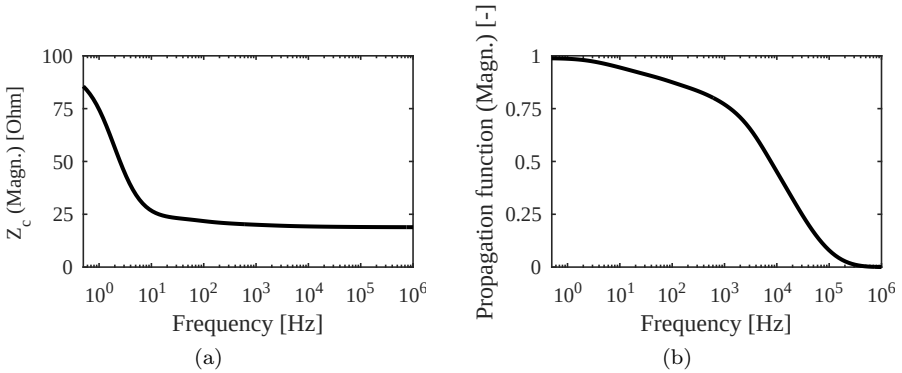


Figure 3.4: Characteristic impedance Z_c (a) and propagation function magnitude for $l = 100$ km (b) for Cable 1.

3.1.4 HVDC Cable Models

In this section, the geometry, materials and modeling assumptions for two cable types used in this work are discussed.

Cable 1: Land Cable

The cable used in Chapter 4 is modeled as a land cable and makes use of the parameters listed in Table 3.1. The cable consists of a copper conductor, XLPE insulation with semiconductor layers (2 and 1 mm for inner and outer layer, respectively), a copper screen and outer insulation. The copper screen is directly grounded at both sides. The parameters of the cable were chosen to attain the properties of the cable described in [30]. The cable burial depth is 1 m and the soil resistivity was set to 100 Ωm. For dc correction in the cable fitting procedure, as described in [114], the shunt conductance of the cable was set to $1{\cdot}10^{-9}$ S/m.

Table 3.2: Cable 2 geometry and material parameters.

	Outer radius [mm]	ρ [Ωm]	ϵ_{rel} [-]	μ_{rel} [-]
Core	19.5	$1.68 \cdot 10^{-8}$	-	1
Insulation	48.7	-	2.3	1
Sheath	51.7	$2.2 \cdot 10^{-7}$	-	1
Insulation	54.7	-	2.3	1
Armor	58.7	$1.8 \cdot 10^{-7}$	-	10
Insulation	63.7	-	2.3	1

Fig. 3.4 shows the resulting cable characteristic impedance and real part of the propagation function for $l = 100$ km. For this cable, the magnitude of the characteristic impedance and propagation speed (evaluated at $f = 1$ MHz) are 18.89 Ω and 167.43 km/ms for the propagation mode between core and sheath.

Cable 2: Submarine Cable

For the HVDC grid test system (explained in detail in Appendix A), XLPE insulated cables suitable for offshore applications were modeled. These models were also used for the test system in Chapter 5.

The parameters for the cable geometry and materials are listed in Table 3.2, and are based on values found in several sources [115, 116, 117, 98]. At the inner insulation layer, semiconductor layers of 1.7 mm and 1.9 mm were modeled, incorporated in the outer radius of the XLPE insulation in Table 3.2. The soil was modeled with a constant resistivity of 1 Ωm, which is a typical value for seawater or wet soil [98].

The voltages in armor and sheath were assumed to be limited due to the close electrical connection of sheath and armor in combination with a semi-wet construction. Consequently, the conductors representing sheath and armor were eliminated. For dc correction in the cable fitting procedure, the shunt conductance of the cable was set to $0.5 \cdot 10^{-10}$ S/m.

Fig. 3.5 shows the characteristic impedance and propagation function for this cable for a length of $l = 100$ km. The magnitude of the characteristic impedance, (evaluated at $f = 1$ MHz) is 33.73 Ω and the wave propagation speed is 183.46 km/ms.

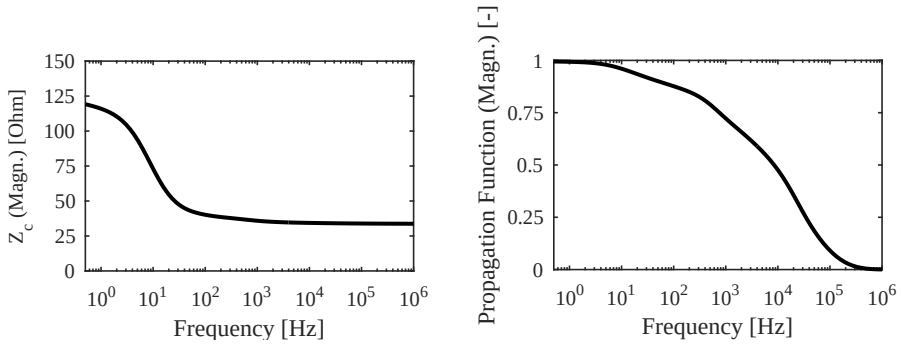


Figure 3.5: Characteristic impedance Z_c (a) and propagation function magnitude for $l = 100$ km (b) for Cable 2.

3.2 Modeling of Half-bridge MMC for Dc Fault Studies

To simulate an MMC in EMT-type software, several types of models with different levels of modeling detail can be used [118]. The most detailed models include a representation of each submodule using either non-linear or linear models for the power electronics, but require considerable computational effort for MMCs with a large number of submodules. Therefore, computationally efficient and reduced models for simulation of MMCs in EMT-type software were developed [119]. Since these models mainly focus on converter control and dynamics, an equivalent circuit model to represent a half-bridge MMC in dc fault studies was developed in this work.

Section 3.2.1 briefly introduces the structure and basic operation of a half-bridge MMC. Next, Section 3.2.2 discusses the modeling assumptions for half-bridge MMCs for the models used in this work. Thereafter, in Section 3.2.3 the fault current provided by a half-bridge MMC is analyzed using a detailed converter model. Based on this analysis, an equivalent circuit model is derived in Section 3.2.4. With the equivalent circuit model, the model complexity is reduced compared with the detailed models, which facilitates dc fault studies. The different models are compared using several case studies in Section 3.3.

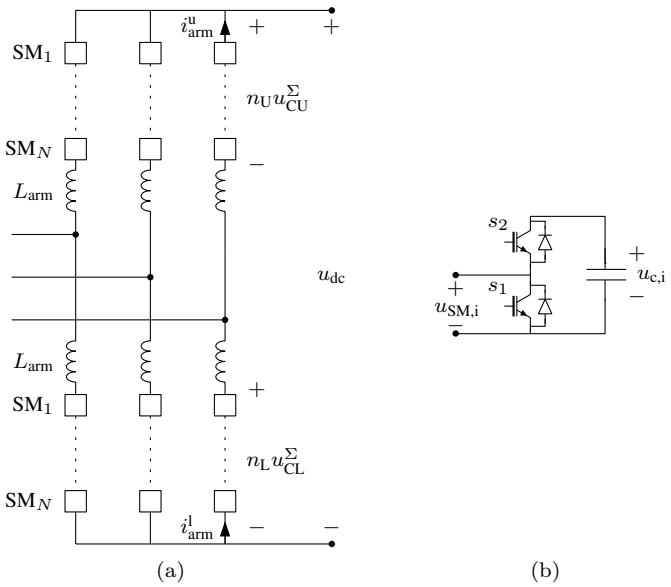


Figure 3.6: Modular multilevel converter topology (a) and half-bridge submodule (b).

3.2.1 Structure and Basic Operation

An MMC has three parallel converter legs which synthesize a three-phase ac voltage out of the dc voltage (Fig. 3.6). The converter legs consist of an upper and lower converter arm, which are a series connection of an inductor (further referred to as arm inductor) and N submodules. For a half-bridge MMC, the submodules include a submodule capacitor C_{SM} and two switch pairs, s_1 and s_2, consisting of an IGBT and an anti-parallel diode.

For each submodule, three main switching states can be defined [36]. If s_1 is closed and s_2 is open, the submodule capacitor is bypassed and the submodule output voltage is zero, i.e., $u_{\mathrm{SM,i}} = 0$. In case s_1 is open and s_2 is closed, the submodule capacitor is in series with the arm and the submodule output voltage is equal to the voltage on the submodule capacitor, $u_{\mathrm{SM,i}} = u_{\mathrm{c,i}}$. In this case, the submodule capacitor charges or discharges depending on the direction of the arm current. In case both s_1 and s_2 are open, current can only flow through the anti-parallel diodes and the submodule is in the "blocked state".

The dc voltage is converted into an ac waveform by varying the number of submodules inserted per arm. The arm output voltages, u_{CU} and u_{CL}, depend

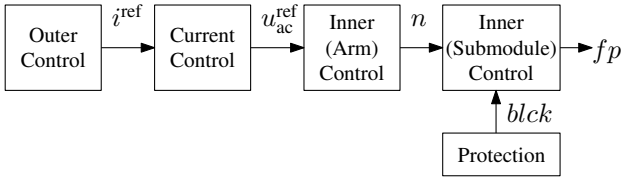


Figure 3.7: Converter control loops, reference signals and internal protection for half-bridge MMC.

on the sum of the capacitor voltages of all submodules in the arm, u_{CU}^{Σ} and u_{CL}^{Σ}, and the fraction of inserted submodules per arm, n_{U} and n_{L}:

$$u_{\text{CU}} = n_{\text{U}} u_{\text{CU}}^{\Sigma} \tag{3.25}$$

$$u_{\text{CL}} = n_{\text{L}} u_{\text{CL}}^{\Sigma}. \tag{3.26}$$

Using the most simple modulation strategy, an ac waveform is obtained by sinusoidally modulating n_{U} and n_{L}:

$$n_{\text{U}} = \frac{1 - m(t)}{2} \tag{3.27}$$

$$n_{\text{L}} = \frac{1 + m(t)}{2}, \tag{3.28}$$

where $m(t) = \hat{m}\cos(\omega t)$ is the per unit ac voltage reference and $\hat{m}$ is a modulation index.

To control an MMC within a HVDC grid, a cascade of control loops is used (Fig. 3.7) [118]. The outer control loops can be set to control the active and reactive power or dc and ac voltage and provide a current reference i^{ref} to the current control loops. With this reference, the current control loops generate an ac voltage reference waveform $u_{\text{ac}}^{\text{ref}}$ for each phase.

The inner (arm) control uses the voltage reference waveform for each phase to generate the insertion indices n for the arm. The modulation strategy using the formulation in (3.27) and (3.28) was shown to result in unwanted internal converter currents, which increase losses and might lead to internal unbalances in capacitor voltages (or arm energies) in case of disturbances [120]. Therefore, alternative modulation strategies and additional inner control loops to control unwanted currents were developed, as discussed in greater detail in [121, 122, 123].

In the last stage, the firing pulses fp for each submodule are generated by the inner (submodule) control, providing energy balancing on a submodule level. The number of submodules inserted per arm can be determined using various algorithms, of which nearest level control is the most simple one [123]. To determine which submodules are inserted, the voltage on the submodule capacitors and the direction of the arm current is considered. Ideally, the total arm voltage is equally shared among the capacitors of the individual submodules. Capacitor voltage balancing control can be done by sorting the capacitor voltages and selecting those submodules to be inserted which have the highest (lowest) voltage in case the current through the arm is positive (negative).

In case of abnormal conditions, the converter internal protection generates a blocking signal *blck* to turn off all IGBTs, overriding the firing pulses generated by the converter control. To detect the abnormal operating condition, several criteria can be used, e.g., arm overcurrent, over- or undervoltage [124]. The IGBTs need to be turned off before the currents exceed the limits from the SOA, as discussed in Section 2.2.2 in Chapter 2.

3.2.2 Modeling of Half-bridge MMC in EMT-type Software

For the studies in this work, two computationally efficient models were used. These models are the detailed equivalent model proposed in [125] and the continuous model proposed in [126]. Below, the modeling assumptions and modeled control loops for each model are discussed.

Detailed Equivalent Model

The detailed equivalent model is mathematically equivalent to an MMC model with linear switches, whereas the calculation time is largely reduced. During normal operation, the switches are modeled as a resistor with low value R^{on} in the "on-state" and a resistor with high value R^{off} in the "off-state". Using the trapezoidal integration rule, a Thévenin equivalent model for the converter arm voltage and resistance, $u^{\text{th,eq}}$ and $R^{\text{th,eq}}$ can be derived, as explained in greater detail in [125]. The calculation time is consequently reduced by representing the submodules of a converter arm as a two-node element in the main circuit and separately calculating the submodule voltages.

If all submodules are in the blocked state, the state of the switches (i.e., the anti-parallel diodes) is determined by the network conditions and can no longer be represented by resistors [127]. To represent the MMC in the blocked state,

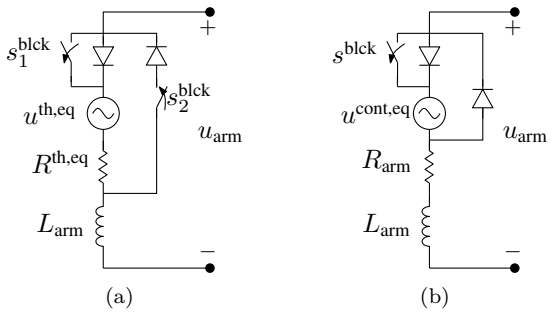


Figure 3.8: Converter arm equivalent model for detailed equivalent model (a) and continuous model (b).

a parallel path must be added to the model. This path consists of a diode for which the resistance is equivalent to the resistance of all series connected anti-parallel diodes (NR^{on}).

Fig. 3.8a shows the circuit of one arm of the detailed equivalent model. During normal operation, switches s_1^{blck} and s_2^{blck} are closed and open, respectively. To represent the blocked state of the converter, they are respectively opened and closed. The control inputs to the detailed equivalent model are firing pulses for every individual submodule and a signal controlling s_1^{blck} and s_2^{blck}.

A comparison of the response to dc pole-to-pole faults at the converter terminals between the detailed equivalent model and a detailed converter model which explicitly represents all submodules, performed in [128] and [129], shows that the former accurately models the response of the converter to dc faults.

Continuous Model with Blocking Capability

The main assumptions in the continuous model are: (i) a high switching frequency compared with the fundamental frequency, (ii) a low resolution of the arm output voltage compared with its amplitude and (iii) internal balance of the submodule capacitor voltages. The first two assumptions are valid for an MMC with a high number of submodules. The latter assumption implies that this type of model is, contrary to the previous one, not suited for the analysis of MMCs on a submodule level.

The continuous model represents the series connected submodules by a voltage source in series with a resistance R_{arm} [126]. The voltage source injects an arm voltage $u^{\text{cont,eq}} = n(t)u^{\Sigma}(t)$, in which $n(t)$ is the fraction of inserted

submodules at t and u^{Σ} represents the sum of the voltages on the submodules. Since individual submodules are not modeled, the total capacitor voltage u^{Σ} is calculated with:

$$u^{\Sigma}(t) = u^{\Sigma}(0) + \frac{n(t)}{C_{\text{arm}}} \int_0^t i_{\text{arm}} dt, \tag{3.29}$$

in which $C_{\text{arm}} = \frac{C_{\text{SM}}}{N}$. The resistance R_{arm} is equal to the sum of the resistances of the power electronics and the resistance of the arm inductor. As in the detailed equivalent model, a parallel path with a bypass diode must be provided to represent the blocked state [126].

The equivalent circuit for one arm of the continuous model is shown in Fig 3.8b. The switch s^{blck} is closed during normal operation and open to represent the blocked state of the converter. The continuous model takes the insertion indices and a signal controlling s^{blck} as control inputs.

In [130], the response of the continuous model to dc pole-to-pole faults was compared with a detailed converter model, and was shown to provide good agreement.

3.2.3 Dc Fault Current Analysis

This section analyzes the fault current of an MMC for a pole-to-pole fault at the converter's dc terminals. To analyze the fault current, a single converter is modeled using the detailed equivalent model with the parameters shown in Table 3.3 (Fig. 3.9). The number of submodules $N = 100$ provides a trade-off between the quality of the output ac waveforms and computational effort of the model. The submodule capacitance was calculated with the formula provided in [131] for a stored energy within the converter capacitance of 40 kJ/MVA, in accordance with the values provided in [36]. The ac system is modeled by a voltage source in series with a complex impedance which determines the short circuit power and X/R-ratio. The converter is connected to the ac system by a transformer with grounded Y-connection at the ac system side and a Δ-connection at the dc system side.

For the outer control loops, dc and ac voltage control in combination with decoupled current control were used. The inner control loops make use of nearest level control and capacitor balancing control as discussed in Section 3.2.1. For this study, circulating current suppressing control was not modeled. In the pre-fault situation, the converter controls the dc voltage to 320 kV and the ac voltage to 185 kV.

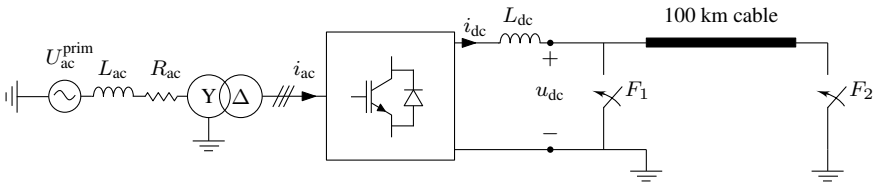


Figure 3.9: MMC test system for fault current analysis.

Table 3.3: Ac system and converter parameters.

Rated power S_{base}	500 MVA
Ac grid voltage $U_{\text{ac}}^{\text{prim}}$	400 kV
Ac converter voltage $U_{\text{ac}}^{\text{sec}}$	185 kV
Transformer leakage reactance	0.1 pu
Ac grid reactance L_{ac}	0.127 H
Ac grid resistance R_{ac}	4 Ω
Nominal dc voltage U_{dc}	320 kV
Submodule capacitance C_{SM}	6500 μF
Number of submodules per arm N	100
Arm inductor L_{arm}	32 mH
IGBT/Diode on-state resistance R^{on}	0.005 Ω
IGBT off-state resistance R^{off}	100 MΩ

Fault Current Stages

To analyze the dc fault current, a pole-to-pole fault is applied at the converter's dc terminals (Fig. 3.9, fault F_1 and $L_{\text{dc}} = 0$ mH). The dc pole-to-pole fault is applied at $t_0 = 25$ ms. To clearly show the different stages in the base case, the IGBTs are turned off 1 ms after fault inception, i.e., at $t_1 = 26$ ms.

Three stages can clearly be distinguished in the development of the dc fault current (Fig. 3.10a). The first stage (stage (i)), in the time interval $[t_0, t_1]$, is characterized by a steep increase of the fault current. The second stage (stage (ii)), in the time interval $[t_1, t_2]$, is characterized by a small increase of the fault current followed by a slow and discontinuous decline of the fault current. In the third stage (stage (iii)), after t_2 =123 ms, the steady-state fault current is reached and the dc fault current is fed solely by the ac system. In Fig. 3.10, t_2 was chosen as the instant after which the dc fault current averaged over 3.3 ms (i.e., one sixth of a cycle at fundamental frequency) does not deviate more than 2% from the averaged steady-state dc fault current.

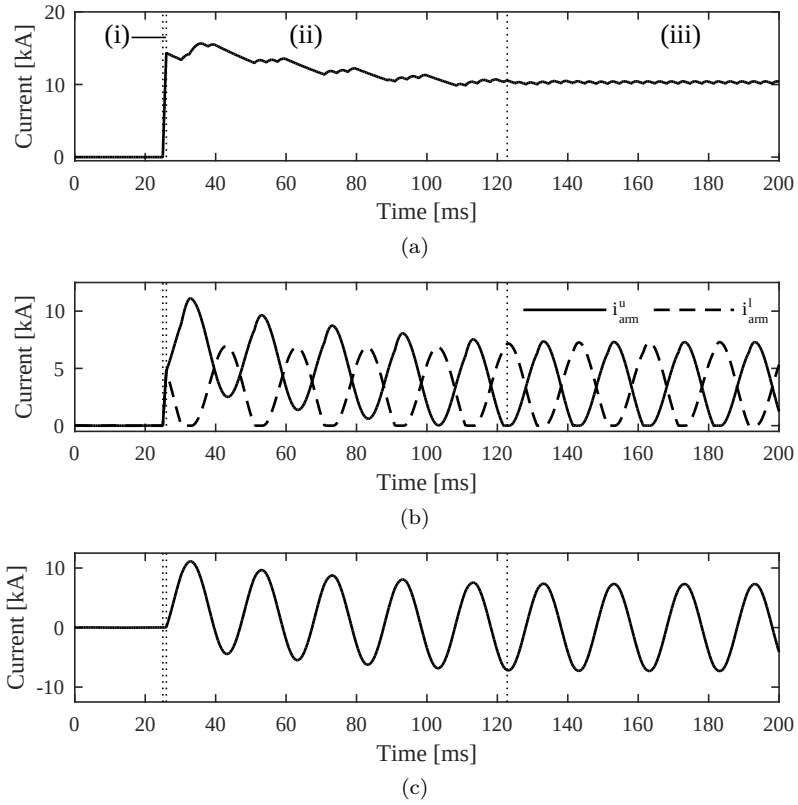


Figure 3.10: Dc current i_{dc} (a), upper and lower arm current, $i^{\mathrm{u}}_{\mathrm{arm}}$ and $i^{\mathrm{l}}_{\mathrm{arm}}$ (b), phase a ac current $i^{\mathrm{a}}_{\mathrm{ac}}$ for solid fault applied at MMC dc terminals (c).

Dc Capacitive Discharge (stage (i)) In this stage, all submodules inserted at t_0 discharge and contribute to the steeply increasing fault current. The upper and lower arm current are nearly identical (Fig. 3.10b), which indicates that the ac infeed during this stage is limited. The capacitors of initially inserted submodules discharge until they are bypassed due to inner control action. Additionally, capacitors from initially bypassed submodules contribute to the steeply increasing fault current if they are inserted during this stage.

Ac Transient Infeed (stage (ii)) The ac transient infeed stage is characterized by ac and dc side phenomena. The second stage starts at the IGBT turn-off instant t_1. In this stage, all submodules are bypassed and all current flows through the IGBT's anti-parallel diodes.

In stage (ii), the dc fault current is the sum of a dc and an ac transient component. The dc transient component is a decaying current due to the release of stored energy in the arm inductors through the anti-parallel diodes. The energy stored in the arm inductors results from the capacitive discharge in stage (i). Due to the ac system model, the ac transient component behaves as the current in a switched RL-circuit driven by an ac voltage source (Fig. 3.10c). In case the ac current exceeds the dc transient component in the arm current, the arm inductors are recharged, e.g., in the interval [30 40] ms (Fig. 3.10a).

Ac Steady-state Infeed (stage (iii)) In this stage, the dc fault current is fed solely by the ac system. The ac fault current is rectified at the dc side through the anti-parallel diodes, resulting in a six-pulse ripple in i_{dc} (Fig. 3.10a). The conduction intervals of the diodes in the upper and lower arm overlap due the arm inductors (Fig. 3.10b).

Effect of the IGBT Turn-off Instant The IGBT turn-off instant separates stages (i) and (ii) and has a major impact on the response of the MMC to dc faults. If $t_1 = 25$ ms, i.e., immediate IGBT turn-off at fault inception, the submodule capacitors do not discharge and the dc fault current is immediately fed by the ac system (Fig. 3.11a). By postponing the turn-off instant to later instants, e.g., 1 or 2 ms after fault inception, the submodule capacitors first discharge into the fault, before the ac system starts to feed in (Fig. 3.11b and c, respectively). The ac contribution in Fig. 3.11 is equal to the sum of the positive ac current in each phase.

3.2.4 Equivalent Circuit Model

The equivalent circuit model for the half-bridge MMC separately models stage (i) and stages (ii) and (iii). First, an RLC-circuit is developed to model a converter leg during stage (i). During this stage, the contribution of the ac system to the dc fault current is assumed to be negligible. Second, an equivalent circuit which is valid for all stages is proposed.

Equivalent RLC-circuit

If the ac infeed is assumed to be negligible during stage (i), the upper and lower arm current, $i^{\mathrm{u}}_{\mathrm{arm}}$ and $i^{\mathrm{l}}_{\mathrm{arm}}$, are identical. Consequently, R_{arm} and L_{arm} of the upper and lower arm are in series (Fig. 3.6). The equivalent leg resistance $R^{\mathrm{eq}}_{\mathrm{leg}}$

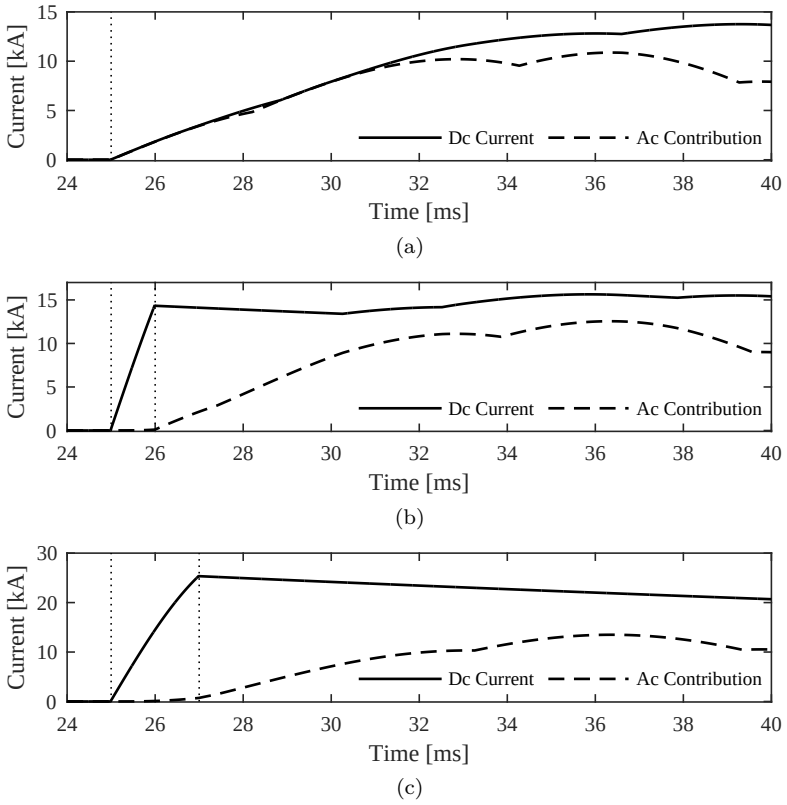


Figure 3.11: Dc current i_{dc} and ac current contribution for various IGBT turn-off instants ($t_1 = 25$ ms (a), $t_1 = 26$ ms (b) and $t_1 = 27$ ms (c)).

and inductance $L_{\mathrm{leg}}^{\mathrm{eq}}$ are therefore given by

$$\begin{aligned} R_{\mathrm{leg}}^{\mathrm{eq}} &= 2R_{\mathrm{arm}}, \\ L_{\mathrm{leg}}^{\mathrm{eq}} &= 2L_{\mathrm{arm}}. \end{aligned} \tag{3.30}$$

The equivalent leg capacitance $C_{\mathrm{leg}}^{\mathrm{eq}}$ depends on the response of the inner controls in case of dc faults. Assuming that during the capacitive discharge, $n_{\mathrm{U}} + n_{\mathrm{L}} \approx 1$, as is the case during normal operation, the equivalent leg capacitance is:

$$C_{\mathrm{leg}}^{\mathrm{eq}} = C_{\mathrm{arm}}. \tag{3.31}$$

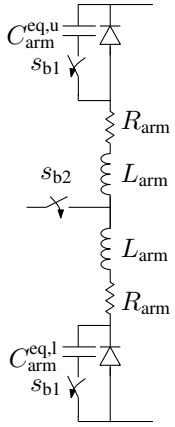


Figure 3.12: Converter leg equivalent circuit.

Consequently, the equivalent circuit model takes into account the change of the total capacitor voltage in a converter leg, since (taking $i_{\text{arm}}^{\text{u}} = i_{\text{arm}}^{\text{l}} = i_{\text{leg}}$)

$$\frac{du_{\text{leg}}^{\Sigma}}{dt} = \frac{(n_{\text{U}} + n_{\text{L}})i_{\text{leg}}}{C_{\text{arm}}} \approx \frac{i_{\text{leg}}}{C_{\text{arm}}}. \tag{3.32}$$

An equivalent RLC-circuit to model a half-bridge MMC during stage (i) is obtained by parallel connection of three equivalent converter leg circuits:

$$R^{\text{eq}} = R_{\text{leg}}^{\text{eq}}/3 \tag{3.33}$$

$$L^{\text{eq}} = L_{\text{leg}}^{\text{eq}}/3 \tag{3.34}$$

$$C^{\text{eq}} = 3C_{\text{leg}}^{\text{eq}}, \tag{3.35}$$

in which R^{eq}, L^{eq} and C^{eq} are the equivalent parameters for the equivalent RLC-circuit which models the converter.

Equivalent converter leg model

The proposed converter leg equivalent circuit is shown in Fig. 3.12. Although not strictly needed, $C_{\text{leg}}^{\text{eq}}$ is divided between upper and lower arm, $C_{\text{arm}}^{\text{eq,u}}$ and $C_{\text{arm}}^{\text{eq,l}}$. The sum of the voltages on these capacitors must be equal to the pre-fault dc voltage. This model represents stage (i) for s_{b1} and s_{b2} in closed and open position, respectively, and stages (ii) and (iii) for the opposite positions of s_{b1}

Table 3.4: Parameters for equivalent circuit model.

Equivalent capacitances $C_{\text{arm}}^{\text{eq,u}}$ and $C_{\text{arm}}^{\text{eq,l}}$	130 μF
Arm inductance L_{arm}	32 mH
Arm resistance R_{arm}	0.5 Ω

and s_{b2}. Initially, s_{b1} (s_{b2}) is in open (closed) position and is closed (opened) at the IGBT turn-off instant. These switches are operated using an external signal.

In contrast with the equivalent converter arm models shown in Fig. 3.8, the submodules in the proposed converter leg equivalent circuit are represented by equivalent capacitors rather than a controlled voltage source. This reduces model complexity of the MMC during fault studies, since no control loops are needed.

In the detailed equivalent model and continuous model, a diode is placed in series with the equivalent sources which allows the submodules capacitors to charge if the pre-fault arm current was negative (Fig. 3.8). In the proposed equivalent circuit, this diode is not modeled as pre-fault conditions are not taken into account.

3.3 Case Studies

The response of the proposed equivalent circuit to dc faults was compared with the one of the detailed equivalent model and the continuous model with blocking capability. For this study, a converter model was developed, using the same parameters and control loops as the ones described in Section 3.2.3. This converter model was used in the same system as shown in Fig. 3.9. Table 3.4 shows the parameters of the equivalent circuit model associated with an MMC with parameters given in Table 3.3.

The cable in Fig. 3.9 is a single cable with a length of 100 km and was modeled using the parameters described in Section 3.1.4 for cable 2.

Three cases were analyzed: (i) solid pole-to-pole fault at the converter terminals, (ii) solid pole-to-ground fault on the cable 100 km from the converter and (iii) solid pole-to-ground fault on the cable located 100 km from the converter with $L_{\text{dc}} = 50$ mH. The IGBTs were turned off 1 ms after the fault is perceived at the converter terminals.

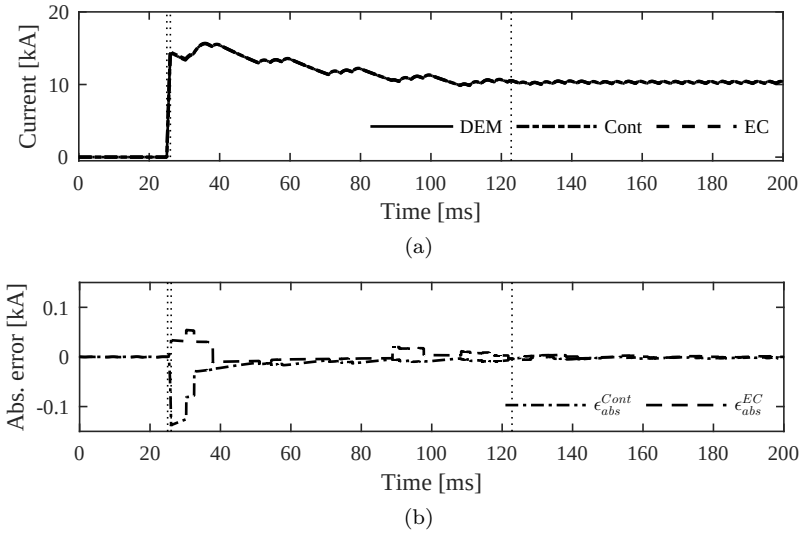


Figure 3.13: Case (i): Dc current i_{dc} for detailed (DEM), continuous (Cont) and equivalent circuit model (EC) (a) and absolute errors $\epsilon_{\mathrm{abs}}^{\mathrm{Cont}}$ and $\epsilon_{\mathrm{abs}}^{\mathrm{EC}}$ (b).

3.3.1 Solid Pole-to-pole Fault at the Converter Terminals

For a solid pole-to-pole fault ($L_{\mathrm{dc}} = 0$) at the converter's dc terminals, the equivalent circuit captures the essential converter fault response during the capacitive discharge as well as ac infeed stage. Clearly, the dc fault current of the equivalent circuit closely follows the ones from the detailed and continuous model (Fig. 3.13a).

The absolute errors between the dc fault current for the detailed equivalent benchmark model, $i_{\mathrm{dc}}^{\mathrm{DEM}}$, and the continuous and proposed equivalent circuit model, respectively $i_{\mathrm{dc}}^{\mathrm{Cont}}$ and $i_{\mathrm{dc}}^{\mathrm{EC}}$, were calculated as follows:

$$\epsilon_{\mathrm{abs}}^{\mathrm{EC}} = i_{\mathrm{dc}}^{\mathrm{DEM}} - i_{\mathrm{dc}}^{\mathrm{EC}} \tag{3.36}$$

$$\epsilon_{\mathrm{abs}}^{\mathrm{Cont}} = i_{\mathrm{dc}}^{\mathrm{DEM}} - i_{\mathrm{dc}}^{\mathrm{Cont}}. \tag{3.37}$$

The maximal absolute error between the dc fault currents of the detailed equivalent model and both the continuous and equivalent circuit model is limited (Fig. 3.13b). The error of the continuous model is negative, indicating that the continuous model overestimates the fault current compared with the detailed equivalent model. For the equivalent circuit model, the error is positive,

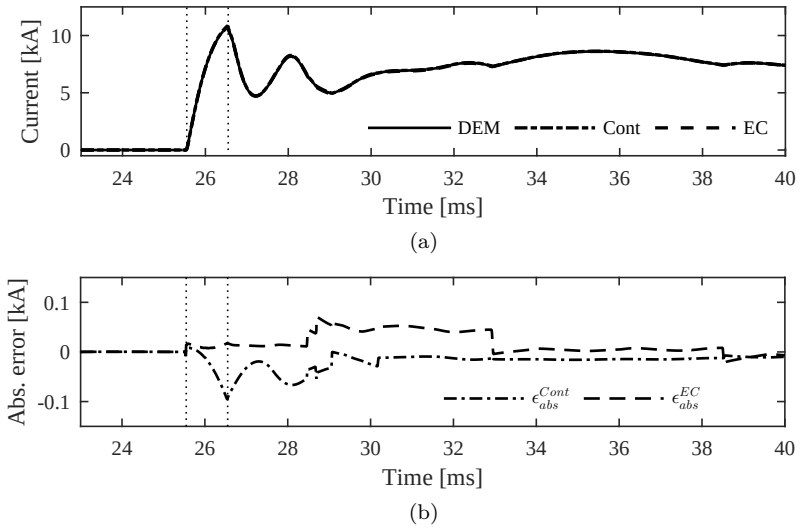


Figure 3.14: Case (ii): Dc current i_{dc} for detailed (DEM), continuous (Cont) and equivalent circuit model (EC) (a) and absolute errors $\epsilon_{\mathrm{abs}}^{\mathrm{Cont}}$ and $\epsilon_{\mathrm{abs}}^{\mathrm{EC}}$ (b).

indicating an underestimation of the fault current compared with the detailed equivalent model.

3.3.2 Pole-to-ground Fault at a Cable

For case (ii), similar to case (i), the differences in dc fault currents and voltages for the three converter models are very small (Fig. 3.14 and Fig. 3.15). In Fig. 3.14, the converter IGBTs are turned off at $t = 26.55$ ms, i.e., 1 ms after the arrival of the fault wave at the converter terminals.

As a consequence, the behavior of the converter as a termination impedance for incoming waves can be approximated by the equivalent RLC-circuit with the parameters of (3.33)-(3.35). This greatly simplifies the converter representation in studies for which mainly the first incident wave is of importance, e.g., protective relaying studies. By increasing the inductance between the converter and cable, the differences between the currents and voltages for each of the converter models further decrease, as shown in Fig. 3.16 and 3.17 for case (iii).

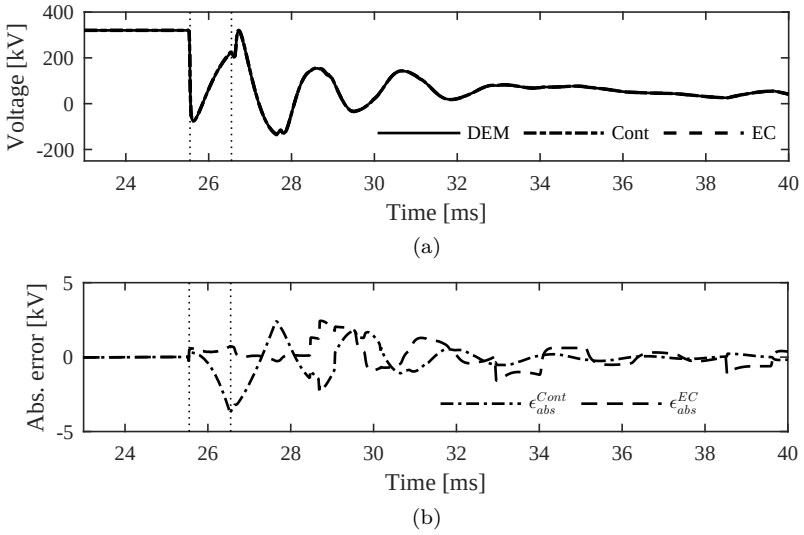


Figure 3.15: Case (ii): Dc voltage u_{dc} for detailed (DEM), continuous (Cont) and equivalent circuit model (EC) (a) and absolute errors $\epsilon_{\mathrm{abs}}^{\mathrm{Cont}}$ and $\epsilon_{\mathrm{abs}}^{\mathrm{EC}}$ (b).

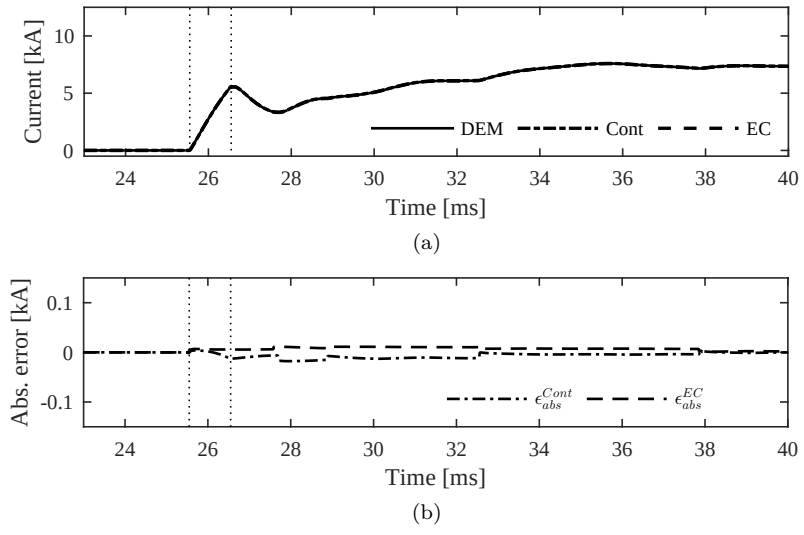
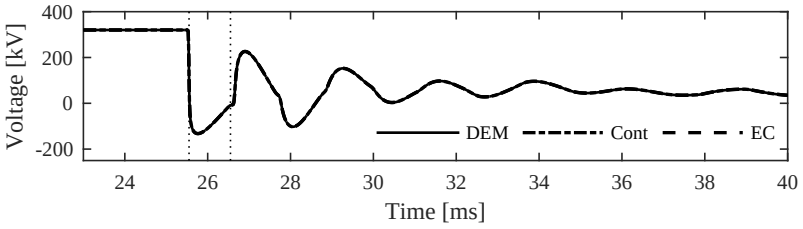
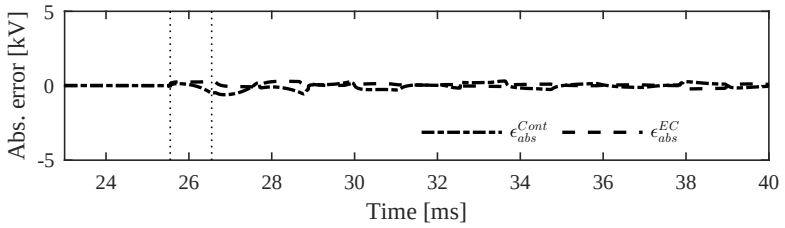


Figure 3.16: Case (iii): Dc current i_{dc} for detailed (DEM), continuous (Cont) and equivalent circuit model (EC) (a) and absolute errors $\epsilon_{\mathrm{abs}}^{\mathrm{Cont}}$ and $\epsilon_{\mathrm{abs}}^{\mathrm{EC}}$ (b).



(a)



(b)

Figure 3.17: Case (iii): Dc voltage u_{dc} for detailed (DEM), continuous (Cont) and equivalent circuit model (EC) (a) and absolute errors $\epsilon_{\mathrm{abs}}^{\mathrm{Cont}}$ and $\epsilon_{\mathrm{abs}}^{\mathrm{EC}}$ (b).

3.4 Conclusion

The preferred cable model for dc fault studies is a frequency-dependent distributed parameters model based on a Norton or Thévenin equivalent circuit which decouples the line ends through the propagation delay. Currently, the most accurate and robust transmission line model available in EMT-type software is the one proposed in [99] and is therefore used for the studies in this work.

The converter models used in this work differ in the level of detail on submodule level. The detailed equivalent model maintains information of each individual submodule, whereas the continuous model lumps together all submodules in a single voltage source. For both models, a parallel path with an anti-parallel diode must be provided to simulate the blocked state of the converter. A comparison of the fault currents of both models for a dc pole-to-pole fault at the converter's dc terminals and at a cable connected to the converter shows the close agreement of the responses of both models.

Since both models were developed from a control perspective, an equivalent circuit model to represent the MMC in dc fault studies was derived based on fault current analysis. The analysis of the dc fault current contribution of the half-bridge MMC shows that the dc fault current can be divided into contributions due to discharge of the submodule capacitors and ac infeed. During the submodule capacitors' discharge, the ac infeed is limited compared with the discharge of the submodules. At the IGBT turn-off instant, the discharge of the submodule capacitors stops and the fault is fed solely by the ac system.

The proposed equivalent circuit largely simplifies the representation of half-bridge MMCs in dc fault studies compared with existing models while maintaining an adequate approximation of the dc short-circuit fault contribution. Due to the absence of control loops in the equivalent circuit, its input requirements and model complexity are several times lower than those of the detailed equivalent or continuous model. A case study including a dc fault at the converter terminals and at a cable connected to a converter shows that the difference in dc fault current contribution by the equivalent circuit model compared with these models is limited.

Chapter 4

Grounding and Configuration of HVDC Grids

*The results of this chapter have been published as "W. Leterme, P. Tielens, S. De Boeck and D. Van Hertem, Overview of grounding and configuration options for meshed HVDC grids, in IEEE Trans. Power Del., vol. 29, no. 6, pp. 2467-2475, Dec. 2014".**

The type of HVDC grid configuration and associated grounding largely impacts system cost (through required equipment ratings), design of protection or future extensibility of the grid. For a HVDC grid, several options exist regarding configuration and grounding. These include a low impedance grounded asymmetric monopolar, a high impedance grounded symmetric monopolar or a low or high impedance grounded bipolar configuration [132]. Moreover, the number of options increases significantly when considering all grounding options such as solid grounding, impedance grounding or leaving the system ungrounded [133].

This chapter provides an overview of options for configuration and dc side grounding of meshed HVDC grids. The impact of grounding and configuration on voltage and current waveforms resulting from a pole-to-ground fault is analyzed using simulations in EMT-type software. The feasibility of using each configuration and associated grounding option as a base configuration

*This paper was the result of joint research by all authors. The explicit contributions of the first author include the development of the model for EMT-analysis and interpretation of the simulation results.

in a meshed HVDC grid is discussed using criteria such as extensibility and flexibility for post-fault operation. Furthermore, the influence of the number and location of grounding points on normal operation and fault behavior of the HVDC grid is investigated.

In Section 4.1, the base configurations and grounding options are discussed. Section 4.2 presents the results of a transient analysis for pole-to-ground faults in point-to-point connections with various configurations and associated grounding options. Next, in Section 4.3, the implications of each configuration and grounding option in a grid are qualitatively discussed with respect to design of protection and post-fault operation. In this section, a case study is used to demonstrate the flexibility of each configuration toward post-fault operation. Finally, in Section 4.4, conclusions are drawn and summarized in Table 4.2.

4.1 Grounding and Configuration of Point-to-point Connections

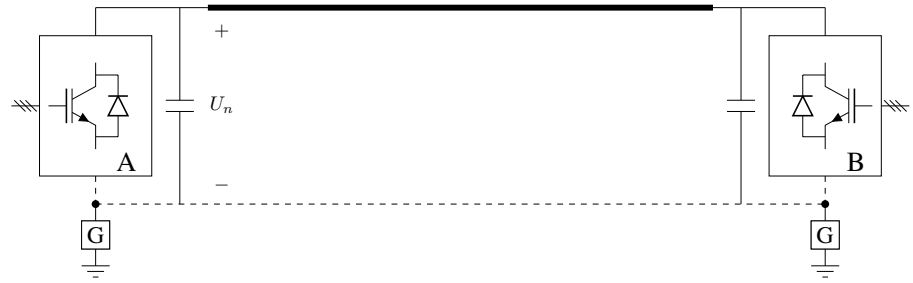
The two base configurations for HVDC are asymmetric and symmetric monopole (Figs. 4.1a and 4.1b). An asymmetric configuration can be extended to a bipolar configuration (Fig. 4.1c). In Fig. 4.1, $\boxed{\text{G}}$ presents the possible grounding locations and can represent any of the basic grounding options, shown in Fig. 4.1d*.

4.1.1 Asymmetric Monopolar Configuration

In normal operation, the positive pole voltage is equal to the nominal voltage of the converter, U_{n}, whereas the metallic return conductor operates at a near-zero voltage (Fig. 4.1a). To limit the voltage on the metallic return, the asymmetric monopole needs to be low impedance grounded with solid grounding as ideal case. To avoid earth currents during normal operation, only one terminal is effectively grounded [5]. In case of a pole-to-ground fault on the positive pole in a solidly grounded system, the steady-state voltage on the metallic return remains near-zero†. The fault current in the positive pole has a high steady-state value in case of converters without fault current blocking capability [134].

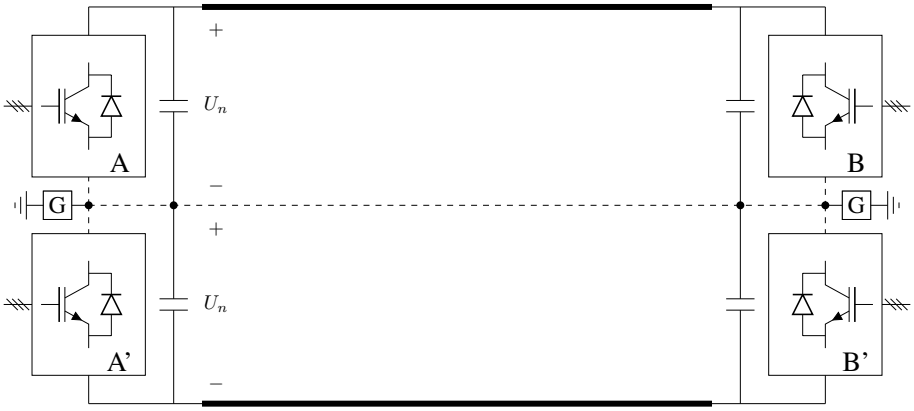
*The distinction between low and high impedance grounding is based on the impedance at low frequencies.

†With steady-state, the prospective steady-state value is meant, i.e., the value occurring when no fault clearing or breakdown of components occurs.

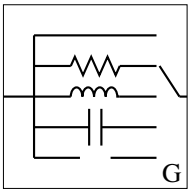


(a) Asymmetric monopolar.

(b) Symmetric monopolar.



(c) Bipolar.



(d) Grounding options.

Figure 4.1: Base configurations and grounding options for point-to-point HVDC connections.

Alternatives for solid grounding are resistance or inductance grounding (Fig. 4.1d). Increasing the grounding resistance decreases steady-state fault currents whereas the steady-state voltage on the metallic return increases. Furthermore, if both converters are effectively grounded, resistance grounding limits the current flowing through the earth during normal operation. An inductor in the ground path does not affect steady-state operation or steady-state fault currents. More advanced grounding schemes, using a combination of impedances or active components at selected grounding locations are possible, however the analysis of these schemes falls out of the scope of this work.

4.1.2 Symmetric Monopolar Configuration

In a symmetric monopolar configuration, the steady-state voltage in normal operation on each pole is half the nominal converter voltage U_n (Fig. 4.1b). A neutral point at the dc side can be made available through large impedances at the dc side, e.g., dc side capacitors. In this work, the possibilities to provide a neutral point at the ac side of the converter, e.g., see [135] and [136], are not considered.

Low impedance grounding (solid, resistance or inductance) as well as high impedance grounding (capacitance, ungrounded) of the neutral point are possible. In case of pole-to-ground faults, the steady-state voltage of the non-faulted pole can reach values up to the converter voltage U_n, i.e., twice the voltage in normal operation. If the grounding is of the low impedance type, the steady-state voltage on the midpoint of the capacitors is clamped to zero in case of faults. The steady-state voltage on the capacitor of the healthy pole is U_n. With high impedance grounding, for pole-to-ground faults, the steady-state voltage on the midpoint of the capacitors is nonzero and the nominal converter voltage U_n is shared between the capacitors. For every grounding type, the steady-state fault current is zero, if the ac system does not provide zero sequence currents and if no surge arresters are used. Surge arresters, e.g., described in [135], limit the overvoltages on the non-faulted pole and provide a path for fault currents in the faulted pole. Compared with a low impedance grounded system, these fault currents are several times lower.

4.1.3 Bipolar Configuration

In a bipolar configuration, two converter are placed in series and each pole is operated at the nominal converter voltage (Fig. 4.1c). For this configuration, low and high impedance dc side grounding are possible. Similar to an asymmetric monopole, the metallic return conductor is operated at near-zero voltage. For a

pole-to-ground fault, in case of solid grounding, the steady-state voltage on the non-faulted pole is the nominal converter voltage U_{n}. The steady-state fault current for a solidly grounded bipolar configuration has similar properties as the fault current for a low impedance asymmetric configuration. Grounding the bipole through a resistor or an inductor is possible as well. Similar conclusions as for the asymmetric configuration can be drawn with regard to fault currents and voltages in case of pole-to-ground faults.

In case of a pole-to-ground fault in a high impedance grounded bipolar configuration, the steady-state voltage on the metallic return can reach the nominal converter voltage U_{n}. Furthermore, the steady-state voltage on the non-faulted pole can reach up to $2U_{\mathrm{n}}$. The steady-state fault current for a single pole-to-ground fault in case of an ungrounded system is zero.

4.2 Pole-to-ground Faults in Point-to-point Connections

This section analyzes the transient waveforms resulting from pole-to-ground faults in HVDC systems using different configurations and associated grounding options as described in the previous section. The parameters for the different grounding types were chosen for demonstration purposes. To enable a clear extraction of the effects of grounding and configuration on a fault transient in a HVDC system, simulations were performed for a point-to-point connection. The insights obtained from these simulations can be used to assess grounding and configuration of meshed HVDC grids. Nevertheless, in meshed HVDC grids, the transient waveforms resulting from a dc fault are also influenced by other factors such as fault location within the grid or grid topology [137].

4.2.1 Test System

For the studies in this chapter, a point-to-point connection consisting of two converters connected by a 400 km cable was considered (Fig. 4.2 for an asymmetric configuration). The HVDC converter topology is the half-bridge MMC topology [39]. In the asymmetric configuration, grounding was provided only at converter 2. A similar model was used for the symmetric configuration, where both converters were grounded in the same manner. For this configuration, capacitors of 100 μF were used to provide the neutral point at the dc side of the converters. Although these capacitors are not strictly needed for MMCs, the cases with and without dc side capacitors were considered for both configurations to analyze the impact on the transient waveforms. In this study, protective

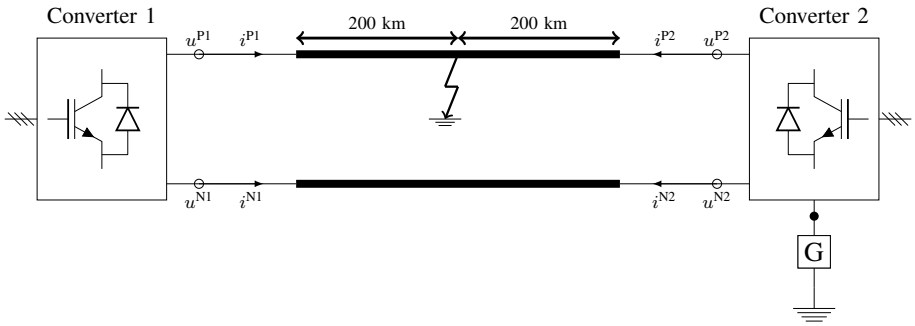


Figure 4.2: Dc side of the test system for the asymmetric monopolar configuration.

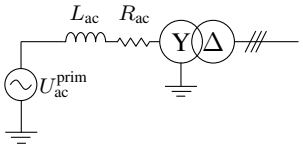


Figure 4.3: Ac system model.

inductors in series with the cables as discussed in [138] were not considered. To interface the converters with the ac systems, the converter transformers have a Yg-Δ winding configuration (Fig. 4.3).

The ac system is modeled by a voltage source and an equivalent grid impedance (Fig. 4.3). For the converters, the detailed equivalent arm model described in Section 3.2.2 of Chapter 3 is used. The grid and converter parameters were based on those found in [30] and [131] and are shown in Table 4.1.

The dc cables use the geometry and material parameters for cable 1 described in Section 3.1.4 of Chapter 3 and were modeled by the frequency-dependent (phase) distributed parameters model [102]. Along with the system grounding, the grounding of the cable screens influences the transient waveforms and should be included in the model. In this study, the screens were solidly grounded at both ends.

In the pre-fault situation, a current of 1 kA flows from converter 2 to converter 1. Converter control was implemented as described in [139]. Converter 1 controls the dc voltage, whereas converter 2 controls the active power. A pole-to-ground fault on the positive pole was simulated by connecting the positive cable conductor to the cable screen and earth. A solid pole-to-ground fault was applied at $t = 1$ ms in the middle of the positive pole, i.e., at 200 km from the

Table 4.1: Grid and converter parameters for the test system.

Ac Primary Voltage $U_{\mathrm{ac}}^{\mathrm{prim}}$	400 kV
Ac Inductance L_{ac}	0.1367 H
Ac Resistance R_{ac}	3.78 Ω
Transformer Ratio	400/185 kV
Transformer Leakage Reactance	0.1 pu
Dc Pole-to-pole Voltage U_{dc}	320 kV
Arm Inductor L_{arm}	15 mH
Number of Submodules	100
Submodule Capacitance C_{SM}	10 mF

converters. Converter IGBTs are blocked when the current through a converter arm exceeds 5 kA.

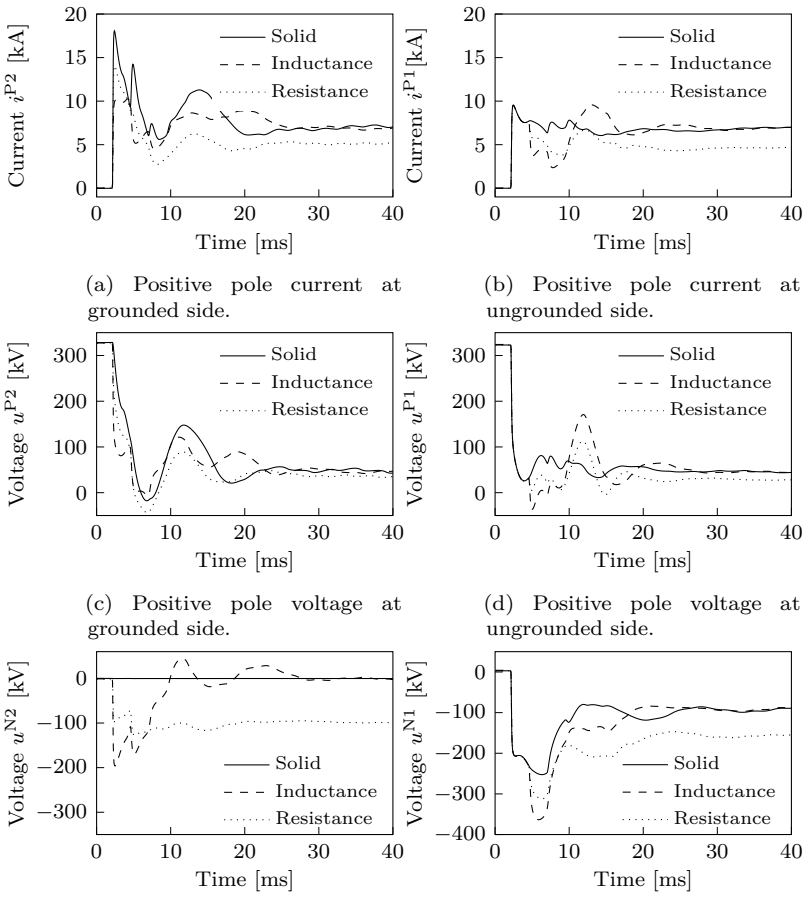
4.2.2 Results

Asymmetric Configuration

The grounding options considered for this configuration were solid grounding (resistor of 1 mΩ), resistance grounding (resistor of 10 Ω) and inductance grounding (inductor of 50 mH). Figs. 4.4 and 4.5 show the currents and voltages measured at the positive pole and the metallic return at both cable ends. Fig. 4.4 includes the case with dc side capacitors, whereas for Fig. 4.5 the dc side capacitors are omitted. In these figures, the currents shown are the fault currents, obtained by subtracting the pre-fault current from the post-fault current.

The current at the grounded converter side increases steeply after the traveling wave caused by the fault reaches the terminal (Fig. 4.4a). At the ungrounded side, the first current peak is half of that of the grounded side because of the difference in line termination (Fig. 4.4b). Moreover, for the first milliseconds after fault inception, the current and voltage waveforms at the ungrounded side are the same for each grounding type (Figs. 4.4b, 4.4d and 4.4f). This is a consequence of the travel time of a wave over the metallic return cable.

The positive pole voltages at grounded and ungrounded side evolve towards a steady-state value close to zero (Figs. 4.4c and 4.4d). There is however a large difference between the negative voltages on the metallic return at the grounded and ungrounded side (Figs. 4.4e and 4.4f). After reaching a minimum value of about -250 kV, the negative voltage at the ungrounded side eventually becomes



(a) Positive pole current at grounded side.

(b) Positive pole current at ungrounded side.

(c) Positive pole voltage at grounded side.

(d) Positive pole voltage at ungrounded side.

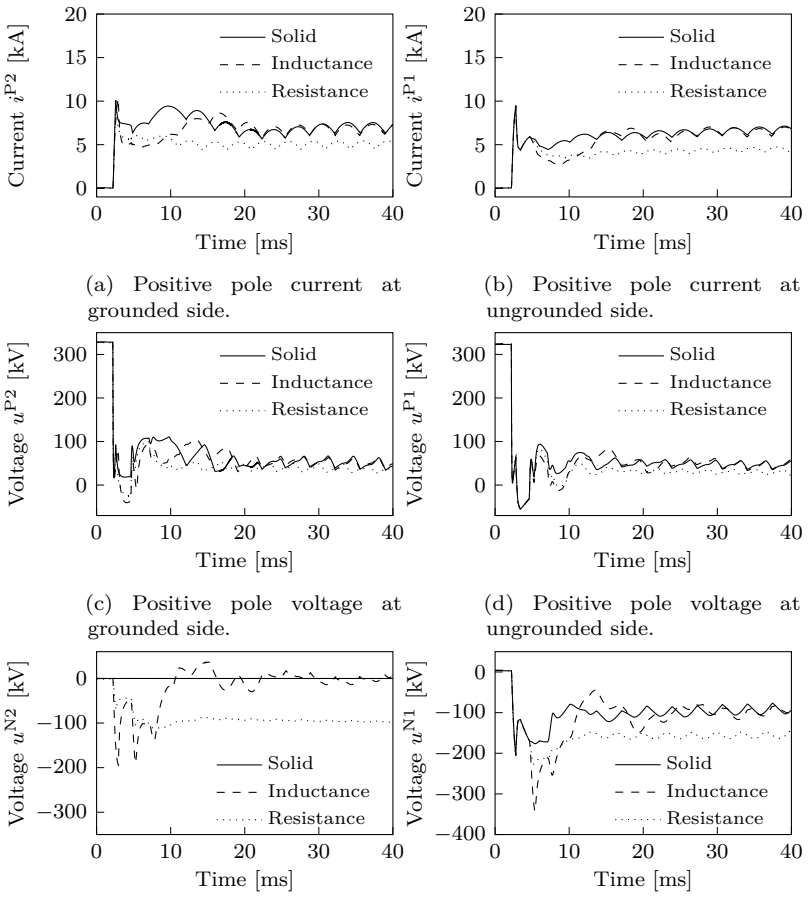
(e) Voltage on metallic return at grounded side.

(f) Voltage on metallic return at ungrounded side.

Figure 4.4: Voltages and currents after a positive pole-to-ground fault for different types of grounding for an asymmetric configuration.

-40 kV because of the voltage drop caused by the fault current flowing over the metallic return cable (Fig. 4.4f).

The type of grounding influences the transient fault behavior as shown in Fig. 4.4. With resistance grounding, the peaks in the transient fault current and the steady-state fault current are lower compared with solid grounding (Fig. 4.4a). However, the steady-state post-fault voltage at the ungrounded side reaches a value around -160 kV (Fig. 4.4f). Even at the grounded side,



(a) Positive pole current at grounded side.

(b) Positive pole current at ungrounded side.

(c) Positive pole voltage at grounded side.

(d) Positive pole voltage at ungrounded side.

(e) Voltage on metallic return at grounded side.

(f) Voltage on metallic return at ungrounded side.

Figure 4.5: Voltages and currents after a positive pole-to-ground fault for different types of grounding for an asymmetric configuration. No dc side capacitors at the converter terminals.

the voltage on the metallic return reaches a value around -100 kV because of the fault current flowing through the grounding resistor (Fig. 4.4e). With inductance grounding, the first peak of the fault current is reduced, whereas the post-fault steady-state currents and voltages take the same values as for solid grounding (Figs. 4.4a and 4.4c). With resistance or inductance grounding, the transient voltage excursions on the metallic return at the ungrounded side

increase compared to those with solid grounding (Fig. 4.4f).

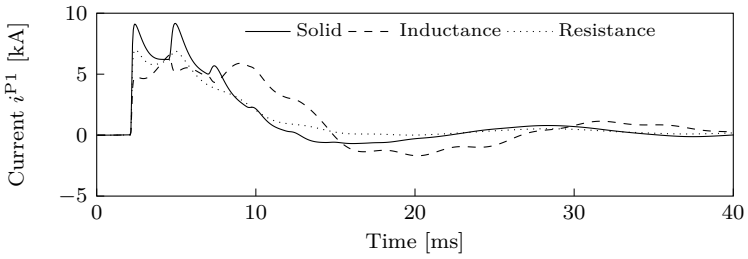
In the case without dc side capacitors, the dc current is initially supplied by the converter submodule capacitors. The initial rate of rise of the current is lower due to the converter arm inductors (Figs. 4.5a and 4.5b). Furthermore, the initial peak current is reduced since turning off the IGBTs stops the discharge of the submodule capacitors. Because of the absence of large dc side capacitors, the dc voltage collapses faster compared with the system with dc side capacitors (cf. Fig. 4.4c and 4.5c). In this case, the type of grounding has a small impact on the peak current but results in voltage excursions on the metallic return which take similar values as in the case with dc side capacitors (cf. Fig. 4.4e and 4.5e).

Symmetric Configuration

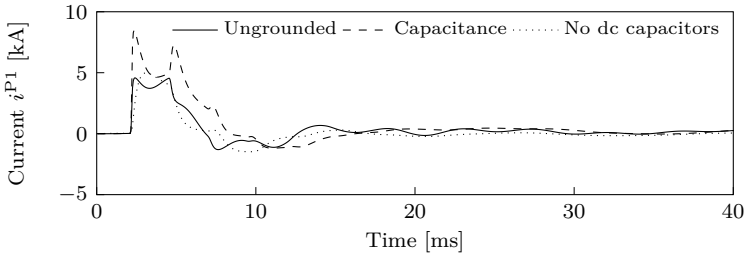
This section discusses the transient waveforms for a pole-to-ground fault in a symmetric configuration for the different grounding options shown in Fig. 4.1. In this case, the pole-to-pole voltage is 320 kV and the pole-to-ground voltage at each pole is 160 kV. The options considered for low impedance grounding are solid grounding, grounding through a resistor of 10 Ω or an inductor of 50 mH (Figs. 4.6 (a) and (c)). For high impedance grounding, a capacitor of 100 μF, high resistance grounding and leaving the system ungrounded are considered (Figs. 4.6 (b) and (d)). Because of the high degree of similarity between the high resistance grounded and ungrounded case, results only from the latter case are presented. As both converters are identically grounded, the voltages and currents at only one terminal are shown.

In case of solid grounding, the current of the positive pole increases steeply after the incidence of the traveling waves caused by the fault because of the discharge of the dc side capacitors of the positive pole (Fig. 4.6a). In the first milliseconds after fault inception, a discontinuity can be noticed in the current waveform each time a traveling wave reaches the terminal. On a longer timescale, the current shows a damped oscillation, eventually decaying to zero. Because of the dc side capacitors, the voltage decay is smooth in comparison with the current (Fig. 4.6c). As expected, the positive and negative pole voltages evolve towards zero and -320 kV, respectively. The transient voltage waveforms show no significant excursions from these voltages (Fig. 4.6c).

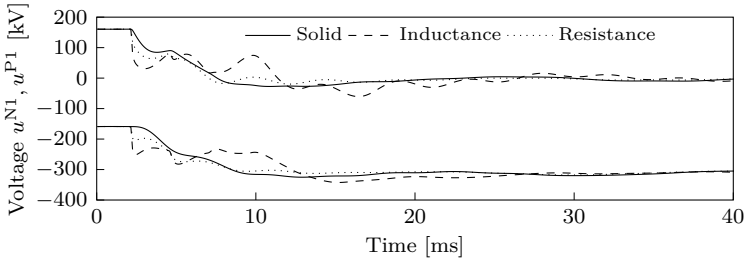
The transient current waveforms are influenced by the type of grounding similar to the asymmetric case. The peak currents are reduced for resistance and inductance grounding compared with the solidly grounded case (Fig. 4.6a). On a longer timescale, the resistance grounding forms an additional damping element in the damped oscillation. With a grounding inductor, the first positive



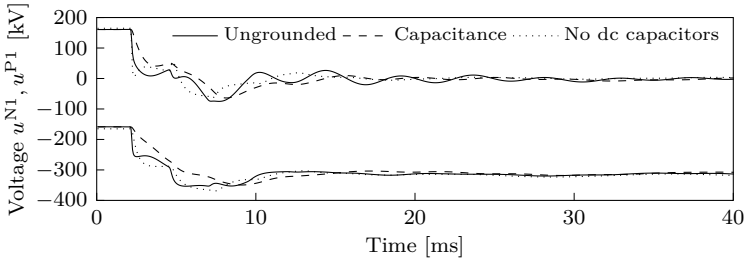
(a) Positive pole currents after a pole-to-ground fault.



(b) Positive pole currents after a pole-to-ground fault.



(c) Positive and negative pole voltages after a pole-to-ground fault.



(d) Positive and negative pole voltages after a pole-to-ground fault.

Figure 4.6: Voltages and currents after a pole-to-ground fault for different types of grounding for a symmetric configuration.

oscillation has a lower maximum value and the frequency of the oscillation changes.

Alternatively, high impedance grounding can be used (Figs. 4.6b and 4.6d). If the dc side capacitors are ungrounded, the main contribution to the fault current is the discharge of the negative pole cable. Therefore, the peak fault current is lower compared to the case with solidly grounded dc side capacitors (Fig. 4.6b). The transient voltage excursions are slightly higher than for the solidly grounded system (Fig. 4.6d).

When grounding through a capacitor, the effective capacitance in case of pole-to-ground faults is decreased since the grounding capacitor is in series with the capacitor between the poles. Consequently, the first peak of the current in the positive pole is slightly decreased compared with solid grounding (Fig. 4.6b). In case the dc side capacitors are omitted, the major contribution to the fault current for pole-to-ground faults originates from the cable discharge. The fault currents and voltages behave similarly to the case with ungrounded dc side capacitors (Figs. 4.6b and 4.6d).

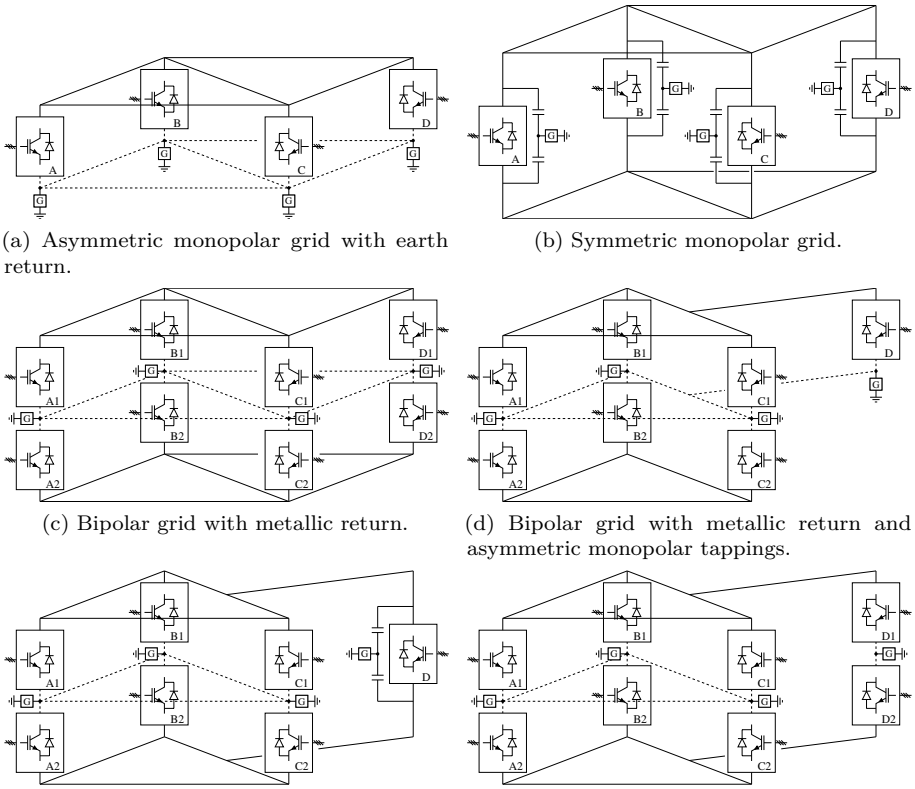
Conclusion of Simulations

For low impedance grounded asymmetric (or bipolar) configurations, in case dc side capacitors are used, the initial peak current after a pole-to-ground fault can be reduced by using resistance or inductance grounding. However, with these types of grounding, the voltages on the metallic return conductor show a larger excursion compared with a solidly grounded system. In case no dc side capacitors are used, the type of grounding does not significantly impact the peak current. The transient voltage excursions on the metallic return in case of resistance or inductance grounding are in the same order of magnitude as those for the case with dc side capacitors.

For a symmetric configuration, similar to an asymmetric configuration, the peak current can be reduced through inserting a resistance or inductance in the grounding path. For this type of configuration, the initial voltage excursions are limited compared with the steady-state voltage on the non-faulted pole, which reaches the nominal voltage.

4.3 Grounding and Lay-out of HVDC Grids

In this section, the base configurations are compared in terms of extensibility and flexibility for post-fault operation. Furthermore, the availability of the



(a) Asymmetric monopolar grid with earth return.

(b) Symmetric monopolar grid.

(c) Bipolar grid with metallic return.

(d) Bipolar grid with metallic return and asymmetric monopolar tappings.

(e) Bipolar grid with metallic return and symmetric monopolar tappings.

(f) Bipolar grid with metallic return and bipolar tappings with earth return.

Figure 4.7: VSC HVDC grid configurations.

different configurations is described.

Beside the type of grounding, the number and location of grounding points in a HVDC grid are discussed, since these have an impact on earth currents. In an European overlay grid, earth currents might need to be avoided as they can endanger human safety, enter the ac grid or entail other impacts on the environment, such as corrosion of nearby metallic constructions [140, 141].

4.3.1 Asymmetric Monopolar Grid

In an asymmetric monopolar grid, low impedance grounding can be provided at every terminal (Fig. 4.7a). In case of a pole-to-ground fault on the positive pole

of any of the links, fault current is supplied through all grounding points. For this type of grids, fast fault clearance is needed because of high fault currents. For post-fault operation, the positive and negative pole of the faulted link are lost and power must be redistributed over other links.

In an asymmetric monopolar grid with multiple effectively grounded points, earth currents will flow in normal operation. These currents can be restricted using resistance grounding. Alternatively, the grid can be low impedance grounded at only one single point and high impedance grounded elsewhere. Several backup grounding points with an active device are required in case of an outage of the effectively grounded point. Moreover, all grounding points need to be dimensioned to sustain the total fault current supplied by all converters. A drawback is different fault behavior in the system depending on the location of the low impedance grounding. Extensive fault studies might be needed for every fault situation and grounding point to determine the settings of protective devices. Additionally, the location of the low impedance grounding influences the voltage rating of cables and converters. In large-scale grids, depending on the power flow, significant voltage drops occur in the system. Converters and cables remote from a grounding point must be rated for operation at these voltages.

A HVDC grid with asymmetric monopolar configuration is extensible with asymmetric monopoles or can be extended to a bipolar configuration.

4.3.2 Symmetric Monopolar Grid

A HVDC grid with symmetric monopolar configuration (e.g., shown in Fig. 4.7b) can be grounded at the midpoint of the dc side capacitors of each converter or left ungrounded at the dc side. For any of the grounding options, the dc side is effectively high impedance grounded. Consequently, no steady-state earth currents flow in normal operation when the system is grounded at multiple locations. Time constraints for the protection of a symmetric monopolar grid can be less stringent compared with an asymmetric monopolar grid as, in case of pole-to-ground faults, there is only a transient fault current. Analogous to the asymmetric monopolar grid, the positive and negative pole of the faulted link are lost in case of faults.

A symmetric monopolar grid is extensible with symmetric monopoles or high impedance grounded bipoles. The converters and transmission lines of every extension must be rated for the nominal converter voltage. This extension cost can be high compared with the power rating of the extension (e.g., a small wind farm).

4.3.3 Bipolar Grid

A HVDC grid with bipolar configuration can be low or high impedance grounded (Fig. 4.7c). Compared with the asymmetric monopolar grid, the power that can be transported over a link is doubled at the cost of one extra cable and a pair of converters. In contrast with a HVDC grid with monopolar configuration, in case of pole-to-ground faults, half of the faulted link is available for power transfer. Therefore, a HVDC grid with bipolar configuration offers a higher flexibility for post-fault operation compared with HVDC grids with monopolar configuration.

A low impedance grounded bipolar grid is comparable to an asymmetric monopolar grid regarding required voltage rating of the poles and fast fault clearance. The bipolar grid can be low impedance grounded at multiple locations. In balanced steady-state operation, no (or only small) earth currents flow. Analogous to the asymmetric monopolar grid, earth currents in unbalanced operation can be limited by resistance grounding or low impedance grounding at only one point.

A low impedance grounded bipolar grid is extensible with other low impedance grounded bipoles or asymmetric tappings between the metallic return conductor and one pole (Fig. 4.7d). The latter option provides a possibility to extend the grid with systems at a reduced cost with respect to a symmetric grid. However, if a bipolar grid is extended with asymmetric tappings, the HVDC grid is continuously operated in unbalanced conditions.

The high impedance grounded bipolar grid is comparable to the symmetric monopolar grid when considering cable voltage ratings, protection requirements and grounding locations. In this case, the metallic return must be rated at the nominal converter voltage. Moreover, if the cable voltage ratings are the same as used for monopolar grids, the nominal converter voltage must be halved compared with monopolar grids.

The high impedance grounded bipolar grid is extensible with other high impedance grounded bipoles, symmetric monopoles (Fig. 4.7e) and asymmetric tappings (Fig. 4.7d). However, insulation requirements of these tappings are higher compared to asymmetric tappings on a low impedance grounded bipolar grid. Finally, a bipolar grid with metallic return cables can be extended by bipolar tappings with earth return (Fig. 4.7f). In case of unbalanced operation, earth currents are possible because of the low impedance grounded bipolar tapping.

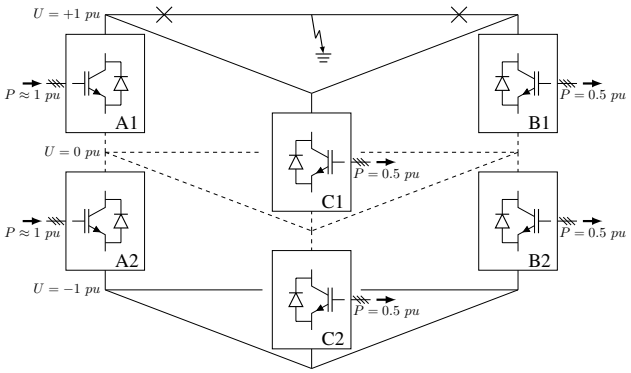


Figure 4.8: Three-terminal bipolar test system.

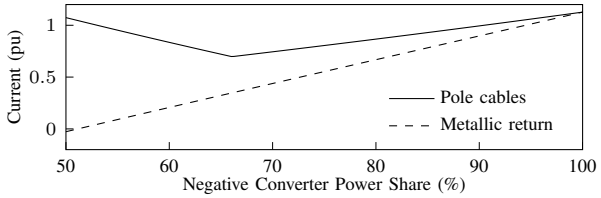
4.3.4 Case Study

The case study illustrates post-fault operation for the different grid types using a three-terminal dc test system (Fig. 4.8). The test system has a bipolar configuration since the results of this configuration for balanced operation are also applicable to monopolar configurations. The converters were modeled as voltage sources and the lines were represented by a resistance of 0.05 pu with base values $U_b = 320$ kV and $P_b = 1000$ MW.

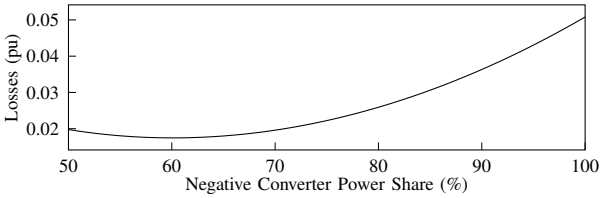
The pre-fault operation settings are shown in Fig. 4.8. Converters A1 and A2 act as voltage regulators and set their voltages to 1 and -1 pu. At terminals B and C, converters B1, B2, C1 and C2 extract 1 pu active power. In the pre-fault situation, the currents in the positive and negative poles between terminals A and B and A and C are equal to 0.5025 pu. The positive and negative poles between terminals B and C and all metallic return conductors carry no current.

Different options for post-fault operation are possible when one of the lines is out of service, e.g., after a pole-to-ground fault. Below two options are presented to operate the HVDC grid after outage of the line between the positive poles of converters A1 and B1. In the first option, balanced operation is continued using the same power settings for each converter as before the fault. In the second option, unbalanced operation through uneven power sharing between positive and negative pole is introduced.

Balanced operation in a bipolar configuration offers no advantage compared with monopolar configurations. In this case, the negative pole between terminals B and C carries no current and power is transported from terminal A to terminal B via terminal C. The rating of the transmission line in the positive pole between



(a) Maximum current.



(b) Network losses.

Figure 4.9: Maximum network currents and network losses as a function of converter power sharing between positive and negative pole.

converters A and C determines the maximal power that can be transferred from converter A to converters B and C.

Through unbalanced operation, the amount of power that can be transferred through the network (considering the same line ratings) can be increased compared with balanced operation. For unbalanced operation, the power of converters B2 and C2 is increased whereas the power of converters B1 and C1 is accordingly decreased. Converters A1 and A2, which regulate the voltage, retain the pre-fault setting of 1 pu voltage. In unbalanced operation, the metallic return conductors start carrying current, whereas the current through the lines is decreased.

To find the optimal amount of power shared between the positive and negative pole, different objectives can be used, e.g., minimization of maximal current in any of the lines or minimization of total network losses. In case the maximal current in any of the lines is minimized, the share of power of the positive and negative pole converters is 33% and 66%, respectively (Fig. 4.9a). In case the negative pole converter's power share is less than 66 %, the maximal line current flows through the positive pole between terminals A and C. In the opposite case, the maximal current through any of the lines flows through the negative poles between terminals A and B and A and C. To minimize the total network losses, the power between positive and negative poles must be shared in a ratio of 40% and 60% (Fig. 4.9b). In a practical application, the unbalanced operation will be limited by the ability of the converters in the non-faulted pole to increase

their power compared with the power flowing in the pre-fault situation.

The degree of unbalanced operation interacts with the type of grounding. For the first option, i.e., balanced operation, multiple converters can be solid or low impedance grounded without significant steady-state earth currents. For the second option, i.e., unbalanced operation, earth currents can flow when multiple converters are effectively low impedance grounded (cf. Fig. 4.9a, the current through the metallic return is nonzero).

4.4 Conclusion

The grounding type and grid configuration have a direct impact on the HVDC grid design and protection as they determine fault current levels and post-fault voltages. Furthermore, the grid configuration has an influence on extensibility of the grid and influences flexibility for post-fault operation. An overview of the impact of grounding and configuration on (i) the fault current and voltage levels and (ii) operation of the HVDC grid is given in Table 4.2.

The analysis of pole-to-ground faults for systems with different configuration and grounding shows that, for low impedance grounded systems, the type and location of grounding affects peak currents and transient voltage excursions. In case of no dc side capacitors, the effect of the dc side grounding on the peak current is limited. For high impedance grounded systems, e.g., symmetrical monopole, the type of dc side grounding mainly influences the peak currents and voltage stresses on components. A case study using a three-terminal test system demonstrates that, through unbalanced operation in a bipolar grid in case of outage of a single pole, available power transfer capacity can be more effectively used compared with monopolar grids.

Table 4.2: Overview of HVDC grid grounding and configurations.

	Asymmetric monopolar grid	Symmetric monopolar grid	Bipolar grid	
Operating voltages[a]	0, U_n	$-U_n/2$, $U_n/2$	$-U_n$, 0, U_n	$-U_n/2$, 0, $U_n/2$
Cables/P[b]	2	2	3/2	3
Grounding type	Low impedance	High impedance[c]	Low impedance	High impedance
Grounding points	Single grounding point Multiple grounding points[d]	Multiple grounding points	Single grounding point Multiple grounding points[d]	Multiple grounding points
Maximum cable voltage[e]	0, U_n	$-U_n$, U_n	U_n, 0, U_n	$-U_n$, $\pm U_n/2$, U_n
Steady-state fault current[e]	Large	Zero	Large	Zero
Extensibility	Asymmetric monopoles Upgrade to bipolar configuration	Symmetric monopoles High impedance grounded bipoles	Low impedance grounded bipoles Asymmetric monopoles between metallic return and pole	High impedance grounded bipoles Asymmetric monopoles between metallic return and pole
Post-fault flexibility after loss of cable	Low	Low	High	High

[a] Pole-to-ground voltage (U_{ptg})
[b] Converter power P $\sim U_{ptg}$
[c] Dc side grounding through dc side capacitors or resistors
[d] Earth currents possible
[e] Considering pole-to-ground faults, prospective values, no protective surge arresters

Chapter 5

Fault Detection in HVDC Grids: Traveling Wave Theory and Signal Processing

*The results of this chapter have been submitted as "W. Leterme, M. Barnes and D. Van Hertem, Fundamental basis and signal processing for traveling wave based fault detection in HVDC grids, CSEE Journal of Power and Energy Systems, 2016".**

Each fault clearing strategy, as described in Section 2.2.3 of Chapter 2, relies on fast fault detection to achieve the required speed of operation. The speed of fault detection depends on the signals used for fault detection on the one hand and on the delay introduced by the measurement unit and the digital filtering needed to discriminate the signal from noise or fault transients not created by dc faults, on the other hand.

In this chapter, traveling wave theory is used to propose general guidelines for the choice of parameters and criteria for fast detection of dc faults in meshed HVDC cable grids. Furthermore, the impact of non-ideal measurements on these methods is investigated and the digital filters that are optimally suited for fault detection in this noisy environment are selected. The approach is demonstrated with a case study on fault detection for a partially selective fault clearing strategy. To this end, a realistically dimensioned HVDC test grid,

*The first author is the main author of the paper. The contributions of the first author include the literature review on fault detection and traveling wave theory, the development of the models in MATLAB and PSCAD and the analysis of the results of the case study.

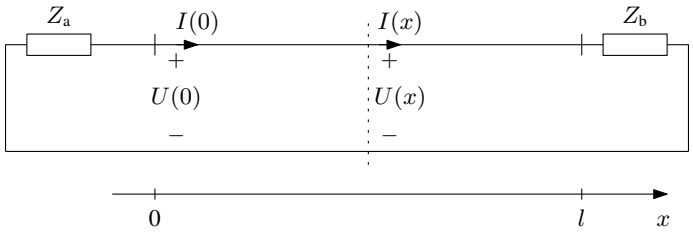


Figure 5.1: Cable of length l with termination impedances Z_a and Z_b.

based on a topology proposed in [142], is used. In [142], a high-level study is performed on the design and economics of a future offshore HVDC system based on independently operated point-to-point or three-terminal systems. In the case study of this chapter, these systems are interconnected to obtain one HVDC grid. To implement a partially selective fault clearing strategy, this grid is divided into two protection zones by fast dc breakers.

First, Section 5.1 briefly recapitulates the parts of traveling wave theory used to determine suitable parameters for fault detection. Next, Section 5.2 proposes the guidelines for the choice of fault detection method. Thereafter, Section 5.3 introduces the models used to analyze the fault transients and Section 5.4 presents the results of the case study. Finally, conclusions are drawn in Section 5.5.

5.1 Traveling Waves

In the first milliseconds after fault inception, the transient voltage and current can be analyzed using traveling wave theory [106]. A fault on a transmission line in a power system causes traveling waves which propagate with a certain speed v on the faulted transmission line. At each discontinuity, these waves are partly reflected back to the fault location, creating a backward traveling wave on the faulted line, and partly transmitted to the rest of the network, creating forward traveling waves on other transmission lines. Consequently, traveling waves created by the fault are attenuated and distorted through propagation and reflections in the network before reaching the protection relay that must detect faults based on these waves.

5.1.1 Propagation over Cables

In the frequency domain, the voltage and current at each location x on a cable can be decomposed in a forward and backward traveling wave, taking the conventions as shown in Fig. 5.1 [143]:

$$U(x) = F_1 e^{-\gamma x} + F_2 e^{\gamma x}, \tag{5.1}$$

$$I(x) = \frac{1}{Z_\mathrm{c}}(F_1 e^{-\gamma x} - F_2 e^{\gamma x}), \tag{5.2}$$

in which F_1 and F_2 are the functions representing the forward and backward traveling wave at $x = 0$ and γ and Z_c are the propagation constant and characteristic impedance as defined in Section 3.1.3 of Chapter 3. F_1 and F_2 are related to $U(0)$ and $I(0)$ as:

$$F_1 = \frac{1}{2}\left(U(0) + Z_\mathrm{c} I(0)\right), \tag{5.3}$$

$$F_2 = \frac{1}{2}\left(U(0) - Z_\mathrm{c} I(0)\right). \tag{5.4}$$

5.1.2 Reflection and Transmission of Traveling Waves

The reflection coefficient Γ relates the forward to the backward traveling wave [106]. At a discontinuity, Γ describes the fraction of the voltage wave that is reflected (assuming that the discontinuity is at $x = 0$, Fig. 5.1):

$$\Gamma = \frac{F_2}{F_1} = \frac{Z_\mathrm{t} - Z_\mathrm{c}}{Z_\mathrm{t} + Z_\mathrm{c}}, \tag{5.5}$$

where Z_t is the surge impedance of the cable termination. The voltage refraction coefficient $T_U = 1 + \Gamma$ describes the fraction of the voltage wave that is transmitted to the rest of the network.

Analogously, the relationship between the incoming and transmitted current wave is given by $T_I = 1 - \Gamma$. The refraction coefficients for typical cable terminations which can be encountered in a HVDC grid are listed in Table 5.1.

For an inductive termination, T_U has a high-pass characteristic whereas T_I has a low-pass characteristic. For high frequencies, T_U and T_I attain a value of 2 and 0, respectively. If the cable termination is capacitive, T_U has a low-pass characteristic, whereas T_I has a high-pass characteristic. For high frequencies, T_I and T_U attain a value of 2 and 0, respectively. For a resistive termination, considering a lossless line, T_U and T_I are independent of frequency. Also in the

Table 5.1: Current and voltage refraction coefficients for various cable terminations.

	Inductor L	Capacitor C	Resistor R	n Cables[1]
T_U	$\frac{2sL}{sL+Z_\mathrm{c}}$	$\frac{2}{sCZ_\mathrm{c}+1}$	$\frac{2R}{R+Z_\mathrm{c}}$	$\frac{2}{n+1}$
T_I	$\frac{2Z_\mathrm{c}}{sL+Z_\mathrm{c}}$	$\frac{s2CZ_\mathrm{c}}{sCZ_\mathrm{c}+1}$	$\frac{2Z_\mathrm{c}}{R+Z_\mathrm{c}}$	$\frac{2n}{n+1}$

[1] Assuming each cable has the same characteristic impedance Z_c.

case where the cable is terminated by n cables with the same characteristic impedance, the refraction coefficients are independent of frequency.

5.2 Fault Detection in HVDC Grids

Protection relays associated with dc breakers must detect a fault within a timeframe of milliseconds to allow faults to be cleared at a current that can still be managed cost-effectively with present breaker technology (cf. Section 2.1.3 of Chapter 2). Within such a timeframe, the voltage and current measured at a relay, $u_\mathrm{r}(t)$ and $i_\mathrm{r}(t)$, can be described by a superposition of the pre-fault voltage and current, u^0 and i^0, and the transient voltage and current caused by the fault, $u'(t)$ and $i'(t)$ [95]:

$$u_\mathrm{r}(t) = u^0 + u'(t) \text{ and} \tag{5.6}$$

$$i_\mathrm{r}(t) = i^0 + i'(t). \tag{5.7}$$

5.2.1 Voltage and Current Magnitude

The most straightforward way to detect faults is to compare the voltage or current magnitude, u_r or i_r, with a certain threshold u^thr or i^thr:

$$u_\mathrm{r} < u^\mathrm{thr} \text{ and} \tag{5.8}$$

$$i_\mathrm{r} > i^\mathrm{thr}. \tag{5.9}$$

Fast fault detection can be achieved by using the voltage and current for a relay at an inductive and capacitive termination, respectively. For fast fault detection

at a resistive termination, voltage or current can be used, since both quantities contain high frequency components.

5.2.2 Voltage and Current Derivative

To discriminate from pre-fault values and to speed up fault detection, the voltage or current derivative can be used:

$$\frac{du_\mathrm{r}}{dt} < du^\mathrm{thr} \text{ and} \tag{5.10}$$

$$\frac{di_\mathrm{r}}{dt} > di^\mathrm{thr}, \tag{5.11}$$

in which du^thr and di^thr are thresholds.

Similar to the voltage and current magnitude, the signals that enable fast fault detection depend on the termination impedance.

5.2.3 Detection Functions

In the literature, several reported discriminant or directional detection functions are based on signals S_1 and S_2, defined as [91, 93, 94, 95]:

$$S_1 = u'(t) - R_\mathrm{c} i'(t) \text{ and} \tag{5.12}$$

$$S_2 = u'(t) + R_\mathrm{c} i'(t), \tag{5.13}$$

in which R_c is used to approximate Z_c by a real value (in this context, R_c is called a "replica surge impedance" in [93]). A common choice for R_c is $R_\mathrm{c} = \lim_{\omega\to\infty} Z_\mathrm{c}$*. Using the conventions of Fig. 5.1, these signals can be used to extract the backward (S_1) or forward (S_2) traveling wave, respectively (cf. Section 5.1.1).

The advantage of a detection function based on (5.12) is its relatively high independency of the network behind the relay for the initial stages of the fault. For a lossless line, S_1 is equal to twice the amplitude of the incoming voltage wave for forward faults whereas it is initially zero for faults in the backward direction [93, 94]. In a practical application, the values for S_1 will deviate from these ideal values due to the mismatch between R_c and Z_c. Furthermore, S_1

*In case $R_\mathrm{c} = \lim_{\omega\to\infty} Z_\mathrm{c}$, S_1 and S_2 correspond to B_i' and B_j' in the weight functions cable model (cf. Section 3.1.4 of Chapter 3).

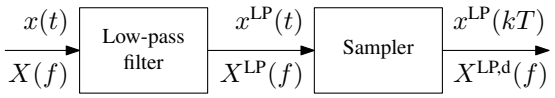


Figure 5.2: Block diagram of the measurement unit electronics.

will not be exactly zero for a fault in the backward direction of the relay. A discussion on the use of S_1 for fault detection is provided in Appendix B.

The transient voltages and currents can be obtained from the measurements by taking the first derivative or by subtracting a delayed version of the measured voltage and current from the instantaneous quantities [91].

5.3 Models

5.3.1 Cables and Converters

The cables are modeled using the Thévenin equivalent for the frequency-dependent distributed parameters model as described in Section 3.1.3 of Chapter 3.

Since for fast fault detection, only the capacitive discharge stage needs to be considered, the converter can be accurately modeled using the equivalent RLC-circuit as described in Section 3.2.4 of Chapter 3. The converter impedance is thus given by

$$Z^{\mathrm{conv}} = R^{\mathrm{eq}} + sL^{\mathrm{eq}} + \frac{1}{sC^{\mathrm{eq}}}, \tag{5.14}$$

where R^{eq}, L^{eq} and C^{eq} are the converter's equivalent resistance, inductance and capacitance.

5.3.2 Measurement Units

As discussed in Section 2.1.4 of Chapter 2, measurement units consist of a primary sensor which converts the primary voltages to a low amplitude signal and electronics which process this signal before sending it to the relays. In this study, the output bandwidth of the measurement units is assumed to be limited by the sensor electronics, as can be assumed for, e.g., an RC-voltage divider or a fiber optic current sensor [72, 144].

Table 5.2: Ac grid and converter parameters.

	OWF A,B,C (D,E)	Onshore A,B (1,2,C)
Rated Power	500 (300) MVA	1000 (500) MVA
Primary voltage	220 kV	400 kV
Secondary voltage	350 kV	350 kV
System X/R	10	10
System SCR	1	10
Transformer leakage reactance	15 %	15%

Table 5.3: Converter parameters.

	OWF A,B,C,D,E, Onshore 1,2,C	Onshore A,B
Submodule capacitance (C_{SM})	1.85 mF	3.7 mF
Arm inductance (L_{arm})	35 mH	50 mH
Arm resistance (R_{arm})	0.5 Ω	0.5 Ω
Series inductance ($L_{\mathrm{s}}^{\mathrm{conv}}$)	10 mH	10 mH
Equivalent capacitance (C^{eq})	55.5 μF	110 μF
Equivalent inductance (L^{eq})	43 mH	53 mH
Equivalent resistance (R^{eq})	0.33 Ω	0.33 Ω

The sensor electronics are modeled by a low-pass filter and analog-to-digital converter (ADC). In this work, a Butterworth low-pass filter with an attenuation of -60 dB at $f_{\mathrm{s}}/2$ is used, where f_{s} is the sampling frequency. This attenuation is used to avoid loss of dynamic range of the ADC for a 10-bit digital signal representation. The cut-off frequency f_{c} of the low-pass filter is determined using (cf. Appendix C)

$$f_{\mathrm{c}} = \frac{f_{\mathrm{s}}}{2} 10^{-\frac{20n}{6B}}, \tag{5.15}$$

in which f_{s} is the sampling frequency, n is the filter order and B is the number of bits. Fig. 5.2 shows the block diagram of the model for the measurement unit electronics. To focus on the delay introduced by the low-pass filter and sampler, a detailed implementation of the quantizer is not considered in the model.

5.4 Case Study

In the case study, fault detection, measurement and digital filtering requirements for protection of the HVDC grid shown in Fig. 5.3 are investigated. This HVDC grid accommodates power transfer from five offshore wind farms (OWF A-E) to two separate onshore networks (connected through converters Onshore A, B and C and Onshore 1 and 2, respectively). The wind farms and onshore networks are connected to one of two hubs, Hub 1 and 2, which are interconnected by a single line. The system configuration is a symmetric monopole with a pole-to-pole dc voltage of 600 kV. All converters are half-bridge MMCs with parameters shown in Tables 5.2 and 5.3. The cable parameters are the ones for Cable 2 as described in Section 3.1.4 of Chapter 3.

To protect the grid with a limited number of fast dc breakers, dc breakers are used only in link L2. These breakers, located close to Hub 2, divide the HVDC grid into two dc protection zones, each encompassing one hub (cf. Section 2.2.3 of Chapter 2). For demonstration purposes, i.e., to focus on fault detection, no breakers were used in link L2 close to Hub 1. The dc breakers must swiftly isolate the healthy from the faulted zone, for dc side faults in any of the protection zones. Consequently, the healthy zone can continue operation, which limits the loss of infeed to an acceptable level for the connected ac networks.

A fast fault detection method for faults in both parts of the network is needed to quickly operate the dc breakers. For fault detection, the voltage and currents are measured at Hub 2 (Fig. 5.4). The current through each line is measured, taking a positive value for current flowing in the direction of the line, and the voltage is measured at the hub ($u_{\mathrm{h},2}$) and cable side of the inductor L_{dc} (u_2). The inductor L_{dc} has a value of 50 mH and is connected in series with the dc breakers CB_2 in L2.

The case study investigates detection of faults F_1, F_2, F_3 and F_4, indicated in Fig. 5.3. All faults are pole-to-pole faults, modeled by a small fault resistance of 0.01 Ω. Faults F_1 and F_3 occur at the converter terminals of converters Onshore A and B. These faults represent the worst case for fault detection in the Hub 1 and Hub 2 protection zones. Faults F_2 and F_4 occur at 25 km from Hub 2 on L2 and L4, respectively. For these faults, the detection speed is important as these occur close to the breakers and consequently give rise to high breaker currents.

In the study, only low impedance faults are considered since these are most probable in cable systems. Although in cable systems, pole-to-pole faults are less probable compared with pole-to-ground faults, in the cases studied and the time frame under consideration, these give rise to similar waveforms in the faulted poles as for pole-to-ground faults. Furthermore, by considering

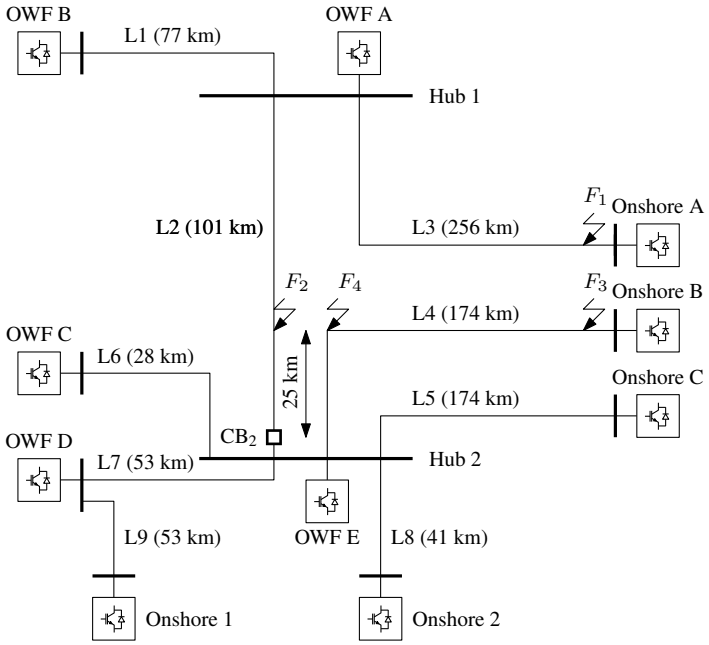


Figure 5.3: HVDC grid topology and faults under study.

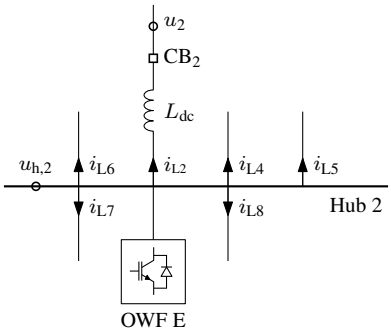


Figure 5.4: Configuration of breaker and voltage and current measurements at Hub 2.

pole-to-pole faults, the results can be generalized to pole-to-ground faults in low impedance grounded systems such as asymmetric or bipolar systems.

5.4.1 Frequency Response

Each fault was analyzed using the magnitude of the frequency response of the transfer functions of the voltage and current at the fault location, U_f and I_f, to the voltage and current at the breaker. The voltage and current at the breaker are U_2 and $I_{\mathrm{L}2}$ for F_1 and F_2, and $U_{\mathrm{h},2}$ and $I_{\mathrm{L}4}$ for F_3 and F_4. An expression for the voltage transfer functions for each fault is given in Appendix D.

Faults in Hub 1 Protection Zone

For both faults, the voltage transfer function has a greater content at higher frequencies than the current transfer function (Fig. 5.5), as the waves are reflected at the series inductor L_dc after traveling over link L2. Furthermore, the magnitude of the frequency response of the transfer function of F_1 exhibits greater attenuation than the one of F_2 for all frequencies. This is caused by two effects: first, the waves from F_1 are reflected at Hub 1, which results in only partial transmission of these waves to Hub 2 and second, the waves from F_1 are attenuated more as these propagate over a longer distance on the cables.

Faults in Hub 2 Protection Zone

For F_3 and F_4, the maximal frequency that is passed through by voltage and current transfer functions is limited by cable attenuation (Fig. 5.6). The magnitude of the frequency response for F_3 is lower than the one of F_4 as F_3 is located further away from Hub 2 than F_4.

5.4.2 Fault Detection Criteria

Faults in the protection zone encompassing Hub 1 were detected with a threshold on the magnitude and derivative of u_2. This enables a high speed of operation by using the high frequency components of the transient voltage at the cable side of the inductor (Fig. 5.5a).

A detection function $dS_{1\mathrm{j}}$ based on (5.12) was used to detect faults in the protection zone encompassing Hub 2, as faults F_3 and F_4 result in transients containing high frequency components in both $u_{\mathrm{h},2}$ and the current through

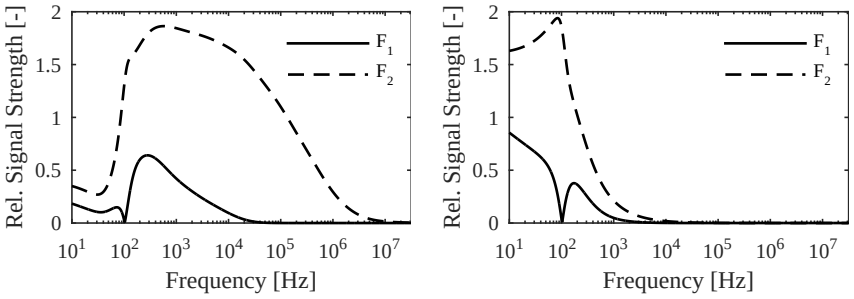


Figure 5.5: Magnitude of the frequency response of U_2/U_f (a) and $I_{\mathrm{L}2}/I_\mathrm{f}$ (b) for F_1 and F_2.

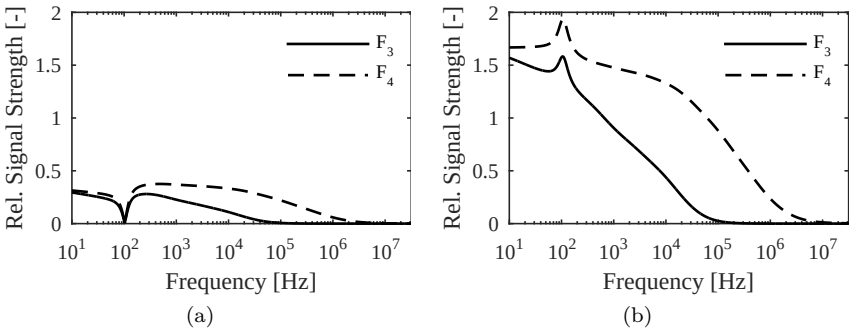


Figure 5.6: Magnitude of the frequency response of $U_{\mathrm{h},2}/U_\mathrm{f}$ (a) and $I_{\mathrm{L}4}/I_\mathrm{f}$ (b) for F_3 and F_4.

links L4-L8 (Fig. 5.6). For the detection function, the first derivative of these quantities was taken to remove the pre-fault offsets:

$$dS_{1,\mathrm{Lj}} = \frac{du_{\mathrm{h},2}}{dt} - R_\mathrm{c}\frac{di_\mathrm{Lj}}{dt}, \tag{5.16}$$

in which i_Lj is the current through link Lj and $R_\mathrm{c} = \mathrm{Re}\left(Z_\mathrm{c}|_{f=1\mathrm{MHz}}\right)$. If $dS_{1\mathrm{j}}$ exceeds a threshold for any of the links L4-L8, CB_2 is tripped.

In summary, the criteria used to trip CB_2 are:

$$u_2 < u_2^{\text{thr}}, \tag{5.17}$$

$$\frac{du_2}{dt} < du_2^{\text{thr}}, \text{ or} \tag{5.18}$$

$$dS_{1,\text{Lj}} > dS^{\text{thr}},\ j \in \{4,5,6,7,8\}. \tag{5.19}$$

Suitable selection of the thresholds allows dc faults to be discriminated from transients not created by dc faults and noise. The threshold u_2^{thr} was set to 80% of the nominal voltage. The thresholds du_2^{thr} and dS^{thr} must be set to avoid false tripping of the breaker due to noise or transients not created by dc faults. These thresholds are set after the measurement units, digital filters and noise level are determined.

5.4.3 Measurement Requirements

This section analyzes the effect of the measurement unit on the speed and sensitivity of the fault detection methods. For all signals used by the selected methods, the maximum frequency is determined by the cable and network characteristics rather than the termination impedance. Therefore, in this section, only F_1 and F_2 are discussed since the analysis of F_3 and F_4 leads to similar results.

For faults close to the relay, information in the high frequency region is lost even for high sampling frequencies up to 500 kHz. As an example, for F_2, with $f_\text{s} = 500$ kHz, the frequency content of the original transfer function is removed in the range of 100 kHz-10 Mhz (Fig. 5.7a). If the sampling frequency is too low, the wavefront of the traveling wave is filtered out, e.g., in Fig. 5.7b, for $f_\text{s} = 10$ kHz. In Fig. 5.7b, the time domain response was obtained for a step input in U_f of -300 kV at $t = 0.005$ ms*:

$$U_\text{f} = -\frac{U^0}{s} e^{-5\cdot 10^{-6} s}, \tag{5.20}$$

where U^0 is the pre-fault voltage (taken as 300 kV) and the corresponding time domain response $u_\text{f}(t)$ is given by:

$$u_\text{f}(t) = -U^0 \theta(t - 5 \cdot 10^{-6}), \tag{5.21}$$

*The transfer function $U_2^{\text{LP}}/U_\text{f}$ was first discretized using zero order hold with a time step of 0.5 μs, before solving the discretized system to obtain the time domain response. Simulations were performed in MATLAB.

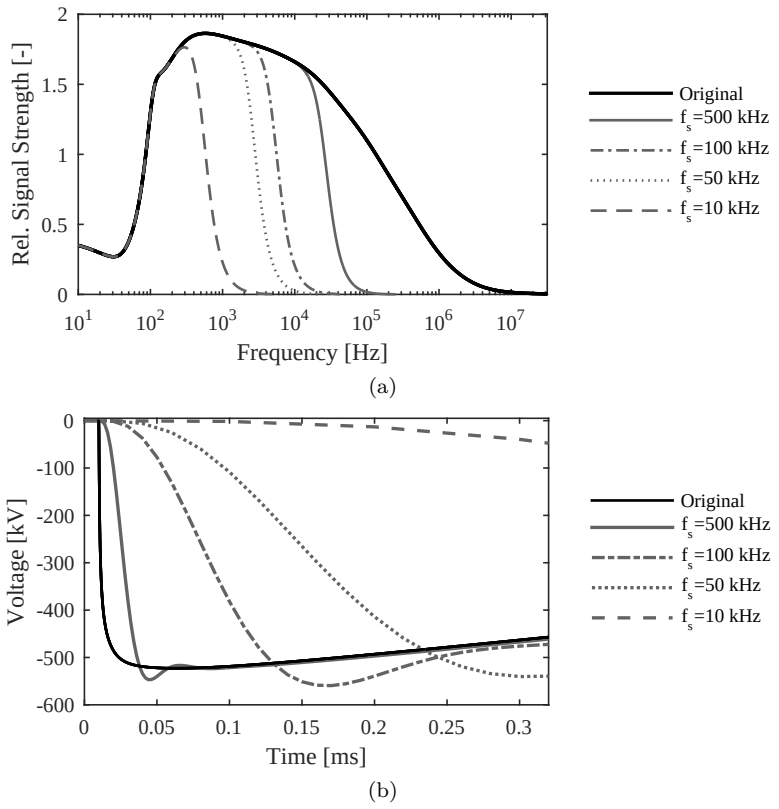


Figure 5.7: Third order Butterworth low-pass filter applied to u_2 for F_2 (Magnitude of the frequency response of $U_2^{\mathrm{LP}}/U_{\mathrm{f}}$ (a) and time response of $U_2^{\mathrm{LP}}/U_{\mathrm{f}}$ for U_{f} given by (5.20) (b)).

in which θ denotes the unit step function.

Compared with a breaker opening time of several milliseconds, the time delay introduced by the low-pass filter on fault detection using (5.17) is insignificant for $f_{\mathrm{s}} > 50$ kHz (for F_2 less than 100 μs), but takes relatively high values (for F_2 between 300 and 400 μs) for $f_{\mathrm{s}} = 10$ kHz (Fig. 5.8). An increase in the order of the low-pass filter only significantly impacts the delay on fault detection of F_1, if $f_{\mathrm{s}} < 50$ kHz (Fig. 5.8). In Fig. 5.8, the time delay introduced by the low-pass filter is defined as the difference between the time instants of fault detection with the original and sampled signal.

Although the voltage derivative decreases with decreasing sampling frequency,

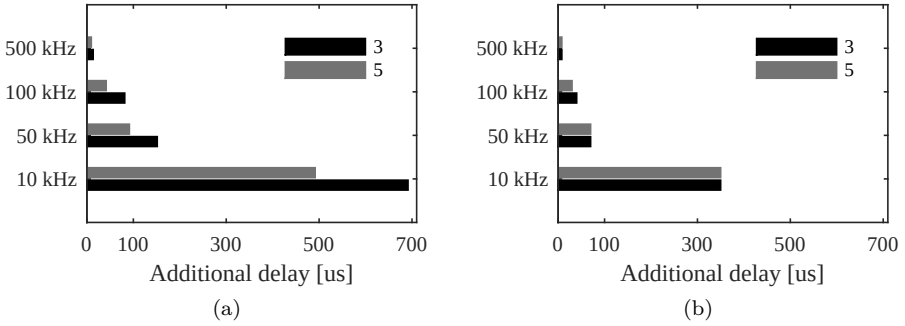


Figure 5.8: Time delay introduced by third and fifth order Butterworth low-pass filter applied to u_2 on fault detection by (5.17) for F_1 (a) and F_2 (b).

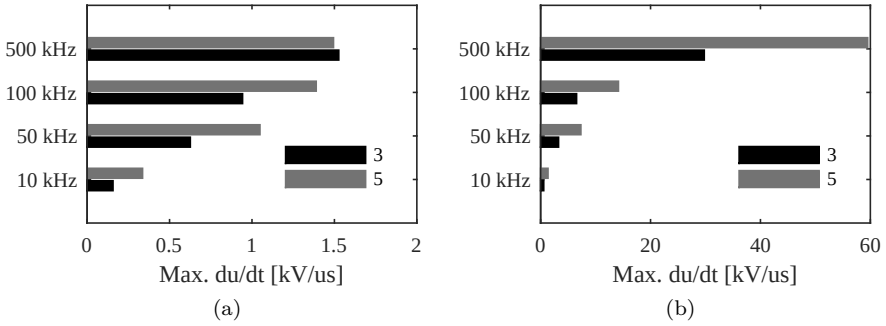


Figure 5.9: Maximal voltage derivative of u_2 for different sampling frequencies and low-pass filters for F_1 (a) and F_2 (b).

it can be used to detect dc faults using sufficiently high (>50 kHz) sampling frequencies. With a third order low-pass filter and a sampling frequency of 50 kHz, the voltage derivative is 0.63 kV/μs for F_1 and 3.27 kV/μs for F_2 (Fig. 5.9). Since the cutoff frequency of the low-pass filter increases with filter order (cf. Section 5.3.2), the maximal voltage derivative for a fifth order filter is in general higher than for the third order filter (Fig. 5.9, except for F_1 at f_s =500 kHz). During normal operation, voltage derivatives within this range ideally do not occur. Nevertheless, dc fault detection using the voltage derivative requires an appropriate digital filter if the signals are corrupted by noise, as described in the next section.

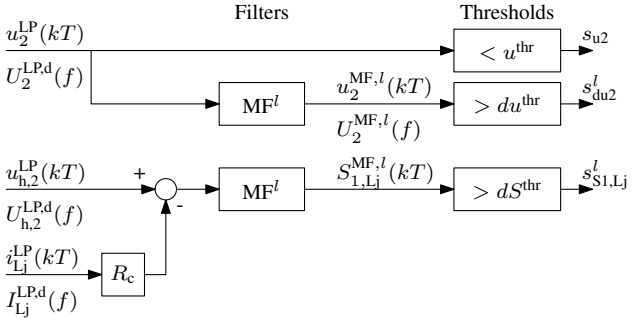


Figure 5.10: Schematic of fault detection.

5.4.4 Matched Filter

To design an appropriate filter for dc fault detection, matched filter theory can be used [145]. The matched filter minimizes the effect of noise on fault detection by maximizing the signal-to-noise ratio (SNR) of its output signal compared to its output noise. For white noise, the impulse response $h(t)$ of the matched filter is

$$h(t) = Cs(t_0 - t), \tag{5.22}$$

in which $s(t)$ is the input signal, C is an arbitrary constant and t_0 ensures causality of the filter [146]. The SNR at the filter output is given by

$$\left(\frac{S}{N}\right)_{\mathrm{out}} = \frac{2E_s}{N_0}, \tag{5.23}$$

in which E_s is the energy of $s(t)$ and $N_0/2$ is the power spectral density level of the noise. For white noise, the SNR of the matched filter can be improved only by increasing the filter length, which increases E_s.

The filter matched for the detection of dc faults is, in digital form,

$$h^l[k] = \begin{cases} -1/\sqrt{l} & \text{for } 0 \leq k \leq l/2 \\ 1/\sqrt{l} & \text{for } l/2 < k \leq l, \end{cases} \tag{5.24}$$

where l is the filter length. The filter is matched to the fault detection signal obtained at the terminal for a fault on a lossless line. This signal is equal to the sum of the pre-fault dc voltage and twice the negative dc voltage for faults in both protection zones (cf. Sections 5.1 and 5.2). In the design of the matched filter, the propagation of the waves over the network is neglected, as it is impossible to match a filter to faults on all locations in the grid.

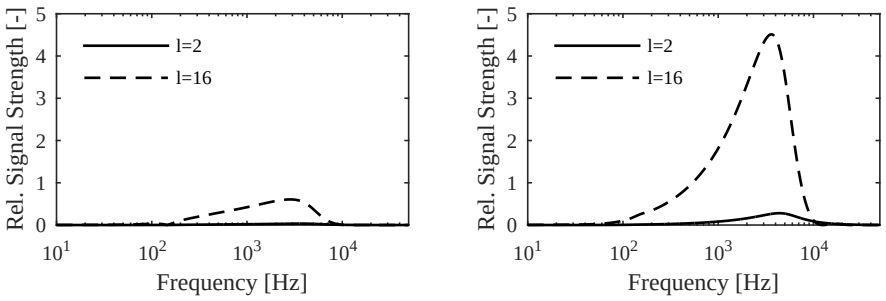


Figure 5.11: Magnitude of the frequency response of $U_2^{\mathrm{MF},l}/U_\mathrm{f}$, with $l = 2$ and $l = 16$, for F_1 (a) and F_2 (b).

A schematic of the fault detection scheme which implements (5.17)-(5.19) is shown in Fig. 5.10. The inputs for the fault detection scheme are the sampled values of u_2, $u_{\mathrm{h},2}$ and i_{Lj}. Since the matched filter is of the form of (5.24), it can be used to implement the criteria based on the first derivative, (5.18) and (5.19). The matched filter outputs are denoted by $u_2^{\mathrm{MF},l}$ and $S_{1,\mathrm{Lj}}^{\mathrm{MF},l}$, where the subscript indicates the filter input and the superscript indicates the filter length. These signals, along with $u_2^{\mathrm{LP}}(kT)$ are presented to the threshold devices. If the output of any of the threshold devices, $s_{\mathrm{u}2}$, $s_{\mathrm{du}2}$ or s_{dir}, becomes one, CB_2 is tripped.

The filter can be matched to faults at various locations by adapting its length l, as shown by Figs. 5.11 and 5.12. With a filter length of 2 samples, the filter output $U_2^{\mathrm{MF},2}$ for F_2 is higher compared with the one for F_1 (Fig. 5.11). This filter is not suited to detect remote faults in a noisy environment as, e.g., for F_1, the filter output $u_2^{\mathrm{MF},2}$ remains below the maximal filter output for white noise associated with a SNR of 40 dB, $n_{\mathrm{max}}^{\mathrm{40dB}}$ (Fig. 5.12a). With a filter length of 16 samples, the filter can be used for detection of close as well as remote faults since for both F_1 and F_2, $u_2^{\mathrm{MF},16}$ exceeds $n_{\mathrm{max}}^{\mathrm{40dB}}$ (Fig. 5.12). For this study, a sampling frequency of 100 kHz and associated third order Butterworth low-pass filter were used.

To evaluate the minimally required SNR for each filter length, a noisy signal associated with an SNR of x dB was generated and its maximum value, $n_{\mathrm{max}}^{\mathrm{xdB}}$, was compared with the maximum value of the filter output for F_1 and F_2 (Fig. 5.10). The filter output for F_1 and F_2 were obtained using the same method as for Fig. 5.12. If $u_2^{\mathrm{MF},l}$ is below $n_{\mathrm{max}}^{\mathrm{xdB}}$, a SNR of x dB is unacceptable. In this study, white Gaussian noise was used to encompass noise introduced through various types of sources, e.g., partial reflections of traveling waves at cable segments, measurement noise, quantization noise, noise due to electronics

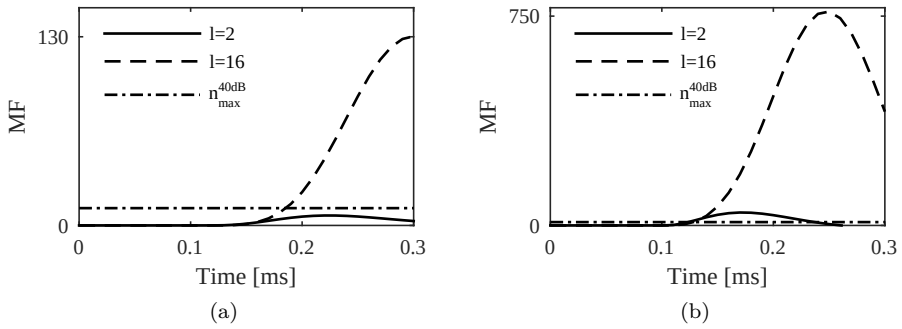


Figure 5.12: Time response $u_2^{\mathrm{MF},l}$ for matched filters of length 2 and 16 applied to u_2 for u_f given by (5.21) and maximum value for 40 dB white Gaussian noise $n_\mathrm{max}^{40\mathrm{dB}}$ for F_1 (a) and F_2 (b).

or noise due to converter switching.

With the matched filters, relatively high noise levels can be tolerated before faults can no longer be detected. Table 5.4 shows the lower limits for the SNR for fault detection of F_1 and F_2 with matched filters in case the measurement output signal is corrupted by white Gaussian noise. The required SNR decreases with increasing filter length or with decreasing distance of the fault to the relay location.

Table 5.4: Required SNR for detection of F_1 and F_2 with matched filters of different length.

l	SNR F_1	SNR F_2
2	47	30
4	37	22
8	30	14
16	22	6

5.4.5 Comparison with PSCAD

In this section, the results obtained with the models of Section 5.3 are verified by PSCAD simulations and the response of the fault detection methods to transients such as those resulting from ac faults is analyzed. Four converters (Onshore A, OWF A, OWF E and OWF C), located close to the fault, were

modeled by a continuous MMC model with anti-parallel diodes, which was verified for dc fault studies in Section 3.3 of Chapter 3. The remote converters were modeled by equivalent RLC-circuits introduced in Section 5.3. All faults occur at $t = 5$ ms and the PSCAD calculation time step used in the study was 1 μs.

For the fault detection methods, the pole-to-ground voltages at both sides of the series inductor L_{dc} and currents through the links L4-L8 were measured. The voltage and current samples were filtered using a third order Butterworth low-pass filter and downsampled to 100 kHz. The threshold on the pole-to-ground voltage, u^{thr}, was set to 240 kV, i.e., $0.8u_{\mathrm{dc}}/2$. To obtain the derivatives for (5.18) and (5.19), matched filters of length 2 and 16 were applied. The thresholds for the derivative criteria were chosen to allow fault detection if the signals are corrupted by white Gaussian noise with a SNR of 40 dB (compared to a voltage level of 300 kV). This led to a threshold value of 11.78 for du_2^{thr} and dS^{thr} (Fig. 5.10).

Faults in Hub 1 Protection Zone

The fault detection signals for faults in the Hub 1 protection zone confirm the result from Table 5.4 that an SNR of 40 dB is not sufficient to detect F_1 with a matched filter of length 2. Fault F_1 is detected using the voltage threshold and the matched filter of length 16, but remains undetected by the filter of length 2 since $u_2^{\mathrm{MF},2}$ remains below 11.78. Therefore, for F_1, s_{du2}^2 remains zero whereas s_{du2}^{16} and s_{u2} indicate fault detection at $t \approx 7$ ms, i.e., the time at which the wave created by F_1 reaches CB_2 (Fig. 5.13a). By contrast, F_2 is detected using the voltage threshold and the matched filters of both lengths. For this fault, all detection signals s become 1 at $t \approx 5.2$ ms, i.e., the time at which the wave created by F_2 reaches CB_2 (Fig. 5.13b).

The time delays for fault detection of F_1 and F_2 are 110 and 45 μs, where the time delay is defined as the difference between the time instant of fault detection and the wave arrival time at the relay. Although F_1 is detected earlier by the matched filters implementing (5.18), the time difference between detection by (5.17) and (5.18) is limited to 30 μs (3 samples).

Faults in Hub 2 Protection Zone

The detection function (5.19) detects F_3 and F_4 with a delay of 45 and 67 μs after the wave arrival time, respectively (Fig. 5.14). Also in this case, the

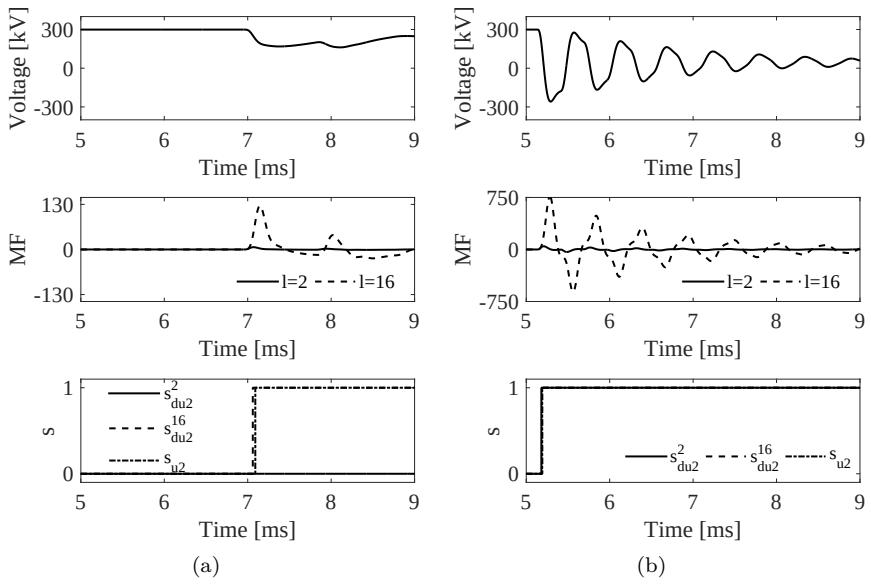


Figure 5.13: Voltage u_2, matched filter output of u_2 for filter lengths 2 and 16 and noise threshold, and fault detection signals for F_1 (a) and F_2 (b).

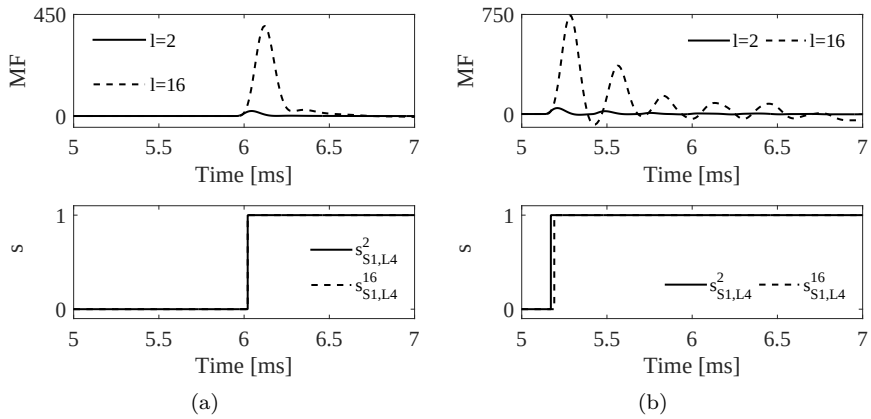


Figure 5.14: Matched filter output for filter lengths 2 and 16 applied to S_1, and fault detection signals for F_3 (a) and F_4 (b).

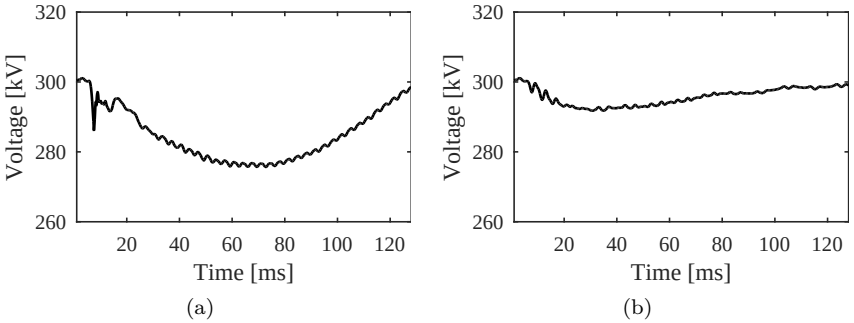


Figure 5.15: Voltage u_2 for $F_{\mathrm{ac,A}}$ (a) and $F_{\mathrm{ac,E}}$ (b).

difference in time delay for the filter of length 16 compared to the one of length 2 is limited, e.g., to 10 μs (one sample) for F_4.

Additionally, the peak value of $S_{1,\mathrm{L4}}^{\mathrm{MF},16}$ for detection of F_4 (Fig. 5.14b) is approximately the same as $u_2^{\mathrm{MF},16}$ for detection of F_2 (Fig. 5.13b). This demonstrates that (5.12) approximately takes a value of twice the incoming voltage wave for forward faults.

Fault Transients Not Created By Dc Faults

With the proposed fault detection methods, transients initiated by three-phase ac faults at converters OWF A and E can be distinguished from dc faults. The three-phase faults, $F_{\mathrm{ac,A}}$ and $F_{\mathrm{ac,E}}$, were applied at $t = 5$ ms at the ac grid side of the converter transformers. As the dc voltage for $F_{\mathrm{ac,A}}$ and $F_{\mathrm{ac,E}}$ remains above 80% of the nominal voltage, i.e., above 240 kV, the ac faults are not detected with (5.17) (Fig. 5.15). With (5.18)-(5.19), ac faults are not detected since, for both cases, the output of the matched filters remain below the threshold selected for a noise level of 40 dB. For instance, in Table 5.5, $u_2^{\mathrm{MF},l}$ for $F_{\mathrm{ac,A}}$ and $F_{\mathrm{ac,E}}$ are one order of magnitude lower than for a noisy signal with SNR 40 dB. By contrast, with a filter length of 16 samples, the filter output for dc faults for the appropriate fault detection criterion is one order of magnitude higher than those for faults not created by dc faults or noise. As an example, for F_3, $S_{1,\mathrm{L4}}^{\mathrm{MF},16}$ is 401.1 compared to 11.78 for the noisy signal.

Table 5.5: Maximum filter outputs (Fig. 5.10) for dc faults and transients not created by dc faults.

Fault type	$u_2^{\mathrm{MF},2}$	$S_{1,\mathrm{L4}}^{\mathrm{MF},2}$	$u_2^{\mathrm{MF},16}$	$S_{1,\mathrm{L4}}^{\mathrm{MF},16}$
F_1	6.65	0.05	126.21	1.05
F_3	0.42	22.35	9.42	401.10
$F_{\mathrm{ac,A}}$	0.15	0.01	2.78	0.29
$F_{\mathrm{ac,E}}$	0.02	0.08	0.52	1.73
Noise with SNR 40 dB	11.78	11.78	11.78	11.78

5.5 Conclusion

Suitable fault detection signals for the fastest fault detection method given a termination impedance can be found by identifying the high frequency content of the transient voltages and currents. In the proposed approach, the frequency content of the waveforms at the relay location is obtained through calculating the transfer function of the voltage and current waves at the relay used for fault detection to the ones at the fault location. The dc fault detection methods designed using the approach can detect dc faults within hundreds of microseconds, which favors fast interruption of the fault current.

Even if the fault detection signals are corrupted by noise, faults can be detected quickly by using a sufficiently high sampling frequency and a matched filter for fault detection. The lower limit on the sampling frequency is found to be in the order of 50 kHz if a 10-bit signal representation and associated low-pass filter are used. Application of matched filter theory for fault detection leads to filters which implement the first order derivative. A case study shows that, with the proposed fault detection criteria and associated filters, the fault detection methods are insensitive towards transients which are not initiated by dc faults, such as faults at the converter ac terminals.

Chapter 6

Non-Unit Protection of HVDC Grids with Inductive Cable Termination

*The results of this chapter have been published as "W. Leterme, J. Beerten and D. Van Hertem, Nonunit protection of HVDC grids with inductive dc cable termination, in IEEE Trans. Power Del., vol. 31, no. 2, pp. 820-828, Apr. 2016".**

The desired properties of a protection algorithm are (i) reliability, (ii) high speed of operation, (iii) simplicity and (iv) insensitivity towards changes in system conditions. For HVDC grid protection, the most stringent requirement is the high speed of operation, with required fault clearing times typically in the order of several milliseconds [147]. Consequently, fast primary protection algorithms for HVDC grid protection are likely to be based on communication-less protection with open protection zones.

In the literature, several protection algorithms for meshed HVDC grids have been proposed. In [27], the protection algorithm developed for selective protection mainly makes use of the current magnitude and its derivative, due to the large fault currents supplied by dc capacitors of two-level converters. For HVDC grids with MMCs or with dc breakers which make use of series inductors, this

*The first author is the main author of the paper. The contributions of the first author include the development of the protection algorithm, the development of the reduced grid model in MATLAB, the sensitivity analysis and comparison of the results with a detailed model implemented in PSCAD.

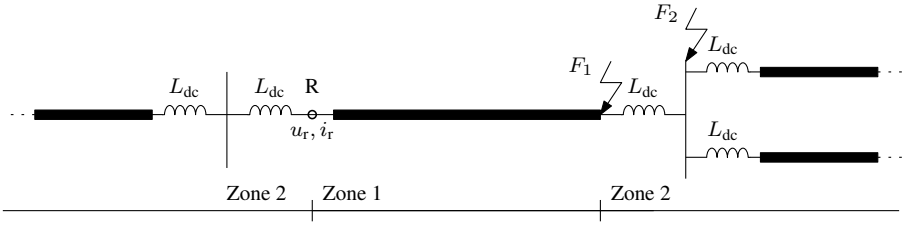


Figure 6.1: Faults within an example grid and protection zones for the relay at R.

assumption is no longer valid. Protection algorithms which employ the series inductors to split the grid into different zones have been proposed in [28, 29, 30]. However, in these works, extensive time domain simulations were used to determine protection thresholds for only specific small scale test systems. A generalized method to determine protection thresholds in large-scale HVDC grids is still missing.

In this chapter, a non-unit protection algorithm for selective HVDC grid protection is developed. First, a set of parameters that characterizes the open protection zone is proposed. Second, a method to determine the thresholds on these parameters is provided. This method makes use of a reduced HVDC grid model, which enables efficient calculation for large-scale HVDC grids with an arbitrary topology while maintaining high accuracy. Third, a sensitivity analysis of the protection thresholds for various parameters, such as grid topology, cable length and series inductor size, is performed. Furthermore, the sensitivity of the protection algorithm towards fault resistance is analyzed.

Section 6.1 builds on the theory introduced in Chapter 5, in particular focusing on the inductive termination, to provide the theoretical background for the protection algorithm. Section 6.2 presents the principles on which the non-unit protection algorithm is based. Section 6.3 introduces the reduced grid model for determining the protection thresholds and discusses the results of the sensitivity analysis. A discussion on measurement requirements based on the conclusions of Chapter 5 is also provided. In Section 6.4, the results obtained by the reduced grid model are compared with a detailed benchmark model.

6.1 Dc Fault Transient Phenomena Involving Inductive Termination

Fig. 6.1 shows a part of a HVDC grid with dc cables terminated by inductors at each end. A relay at location R is shown for the dc cable. For non-unit protection, this relay must discriminate faults on the cable to be protected (e.g., F_1) from faults external to the cable (e.g., F_2) using local measurements u_r and i_r (where the positive direction of i_r is in the direction of the cable to be protected). The non-unit protection algorithm developed in this chapter makes use of the waveforms associated with the first incident traveling wave to discriminate these faults.

For the reflection of the first incident wave from faults at F_1 and F_2, the transient component of the voltage and current measured at R, respectively U_r and I_r, can be described as follows (see Appendix D):

$$U_\mathrm{r} = (1+\Gamma)HU_\mathrm{f}, \tag{6.1}$$

$$I_\mathrm{r} = (1-\Gamma)HI_\mathrm{f}, \tag{6.2}$$

where Γ is the reflection coefficient, H represents the wave propagation over the cable, and U_f and I_f are the voltage and current on the cable at the location of the fault.

Voltage and Current Wave at the Fault Location

For protection algorithms making use of the first incident wave, U_f or I_f are the only variables in (6.5) and (6.6) which can be used to discriminate forward faults at the cable side of the series inductor, F_1, from faults behind the series inductor, F_2 (Fig. 6.1)*. The worst case for discriminating both faults is a fault F_1 with a certain resistance and a solid fault F_2. To simplify the analysis at this stage, fault F_1 is considered to occur before the cable end. If a fault occurs, the voltage at the fault location changes from the pre-fault voltage to zero. This voltage change, described by voltage source U'_f, is divided over the fault resistance and the cable characteristic impedance according to

$$U_{\mathrm{f},F_1} = \frac{Z_\mathrm{c}/2}{R_\mathrm{f} + Z_\mathrm{c}/2} U'_\mathrm{f}, \tag{6.3}$$

in which R_f is the fault resistance and the factor $1/2$ accounts for the fact that the fault resistance is in series with the characteristic impedances of the cable

*Throughout this chapter, the faults F_1 and F_2 refer to the faults at the cable end and faults behind the series inductor, respectively.

at both sides of the fault. For a solid fault F_2, a similar relationship is found between U'_{f} and the voltage wave at the cable U_{f,F_2}. In this case, the voltage at the fault location U'_{f} is divided over the cable and the inductor:

$$U_{\mathrm{f},F_2} = \frac{Z_{\mathrm{c}}}{sL_{\mathrm{dc}} + Z_{\mathrm{c}}} U'_{\mathrm{f}}, \tag{6.4}$$

in which L_{dc} is the inductance of the series inductor and Z_{c} is the characteristic impedance of the cable. The difference between (6.3) and (6.4) lies in the pole caused by the series inductor L_{dc}. The transfer function described in (6.4) has a low-pass characteristic, whereas the one described in (6.3) exhibits a constant attenuation for all frequencies. Consequently, the wavefront for traveling waves created by fault F_2 will be less steep compared with those created by fault F_1.

Reflection at an Inductive Termination

For a purely inductive cable termination, the time domain solution for the voltage and current at the relay is given by (considering a lossless cable with characteristic impedance Z'^{*}_{c} and neglecting the time delay due to wave propagation):

$$u'_{\mathrm{r}} = 2e^{-t/(L_{\mathrm{dc}}/Z'_{\mathrm{c}})} u_{\mathrm{f}}, \tag{6.5}$$

$$i'_{\mathrm{r}} = 2(1 - e^{-t/(L_{\mathrm{dc}}/Z'_{\mathrm{c}})}) i_{\mathrm{f}}, \tag{6.6}$$

where u_{f} and i_{f} are the amplitude of the incident voltage and current wave and $i_{\mathrm{f}} = -u_{\mathrm{f}}/Z'_{\mathrm{c}}$.

Consequently, for a lossless cable, u'_{r} is at $t = 0$ equal to twice the incident voltage wave. The current i'_{r} is at $t = 0$ zero and increases with a time constant defined by the ratio $L_{\mathrm{dc}}/Z'_{\mathrm{c}}$.

Fig. 6.2 illustrates the reflection of the first incident voltage and current wave at a purely inductive termination for F_1 (for $R_{\mathrm{f}} = 0$ and $R_{\mathrm{f}} = Z'_{\mathrm{c}}/2$) and F_2 ($R_{\mathrm{f}} = 0$), considering a lossless cable. The difference between F_1 and F_2 can be clearly noticed in u'_{r}. For F_2, u'_{r} shows a continuous and less steep decline compared with u'_{r} for F_1, which exhibits a discontinuous jump at $t = 0$.

*The characteristic impedance can be taken as, e.g., $Z'_{\mathrm{c}} = \lim_{\omega\to\infty} Z_c$ (cf. Section 3.1.3 of Chapter 3) or should be evaluated at a high frequency (e.g., at 1 MHz).

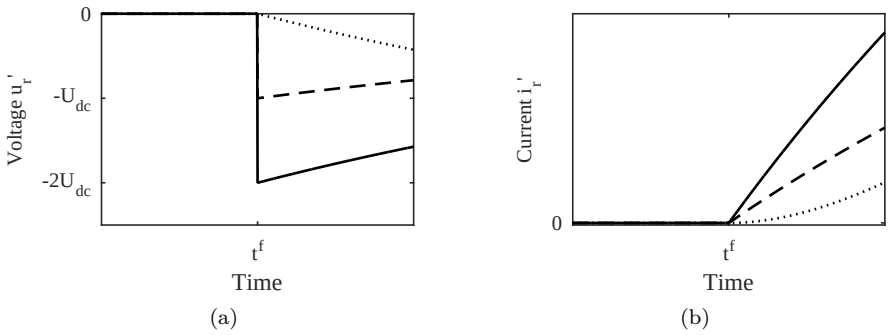


Figure 6.2: Voltage (a) and current (b) for fault waves reflected at inductive terminal (solid line: F_1, $R_\mathrm{f} = 0\ \Omega$, dashed line: F_1, $R_\mathrm{f} = Z'_\mathrm{c}/2$, dotted line: F_2, $R_\mathrm{f} = 0\ \Omega$).

6.2 Non-Unit Protection Algorithm

The proposed non-unit protection algorithm follows a two-stage approach. In the first stage, the protection algorithm detects the fault. Thereafter, in the second stage, the protection algorithm determines the zone in which the fault is located.

6.2.1 Protection Zones

Fig. 6.1 shows the protection zones for the proposed non-unit protection algorithm. The primary protection or first zone is bounded by the series inductors terminating the protected cable. The relay must instantly trip its associated breaker for a fault within this zone. For faults outside this zone, the relay must refrain from instantly tripping its associated breaker, but can be used to provide backup protection. Faults outside this zone are assumed to be in the relay's second zone. In this chapter, the boundaries of the second zone are not considered.

6.2.2 Fault Detection

The protection algorithm is initiated by a starting function that is used to detect dc side faults. Beside the required speed of operation, the main requirement for the starting function is dependability as the protection algorithm must be initiated for every possible fault, i.e., for faults in the first as well as the second

zone. For cables with an inductive termination, as discussed in Section 5.2 of Chapter 5, faults can be swiftly detected using an undervoltage criterion:

$$u_{\mathrm{r}} < u^{\mathrm{thr,d}}. \tag{6.7}$$

In (6.7), $u^{\mathrm{thr,d}}$ must be set to discriminate between faults and normal operation. The time for fault detection t^{d} depends on the location of the fault. Faults in the first zone are detected faster than those in the second zone, as the voltage derivative for faults in the second zone is lower compared with those in the first zone due to the series inductors terminating the cable (Fig. 6.2).

6.2.3 Fault Discrimination

In the second stage the protection zone in which a fault occurs must be identified to guarantee selective tripping. In this stage, security is important since a breaker must only be tripped instantly for faults occurring in the first zone.

Considering Figs. 6.1 and 6.2, the discrimination of forward faults F_1 and F_2 is most clear in the voltage. This is due to the inductive termination at R, which causes voltage waves to be reflected with the same polarity and current waves to be reflected with opposite polarity. Consequently, the first proposed criterion to discriminate forward faults is based on the derivative of u_{r}.

To increase robustness of the relaying algorithm considering measurement errors and noise, an additional undervoltage criterion is proposed. The undervoltage criterion is achieved by monitoring the voltage for a defined period of time $\Delta t^{\mathrm{discr}}$ after fault detection. This criterion must be considered independently from the voltage derivative criterion, as in some cases, both criteria will not be satisfied at the same time.

With the criteria above, faults in the forward direction cannot be discriminated from those in the backward direction of the relay. Therefore, the current derivative is used to discriminate between forward and backward faults. The sign of the current derivative determines the fault direction: a positive or negative sign indicates a forward or backward fault respectively. In summary, the first and second zone can be defined as:

$$\begin{aligned} \text{First zone} &\begin{cases} \frac{du_{\mathrm{r}}}{dt} < du^{\mathrm{thr,1}} \\ u_{\mathrm{r}}(t^{\mathrm{d}} + \Delta t^{\mathrm{discr}}) < u^{\mathrm{thr,1}} \\ \frac{di_{\mathrm{r}}}{dt} > 0 \end{cases} , \\ \text{Second zone} &\begin{cases} \frac{du_{\mathrm{r}}}{dt} > du^{\mathrm{thr,1}} \\ u^{\mathrm{thr,1}} < u_{\mathrm{r}}(t^{\mathrm{d}} + \Delta t^{\mathrm{discr}}) < u^{\mathrm{thr,d}} \end{cases} , \end{aligned} \tag{6.8}$$

in which $du^{\mathrm{thr},1}$ is a threshold on the voltage derivative and $u^{\mathrm{thr},1}$ is a threshold on the voltage.

The total time for the protection algorithm consists of the fault detection time $t^{\mathrm{d}} - t^{\mathrm{f}}$, where t^{f} is the time instant of fault inception, and the fault discrimination time $\Delta t^{\mathrm{discr}}$. The fault discrimination time $\Delta t^{\mathrm{discr}}$ must be fixed to a small value since, also for second zone faults, the voltage keeps decreasing in time (Fig. 6.2).

6.3 Protection Thresholds

This section deals with the determination of the protection thresholds for the principles proposed in the previous section. To this end, a reduced grid model is first developed. The reduced model can be used for fault analysis to determine the thresholds of (6.8). Thereafter, a sensitivity analysis on these thresholds is performed.

6.3.1 Reduced Grid Model

The focus of the reduced grid model lies on fault detection and discrimination based on the first incident fault wave, thus it needs to be accurate for the first milliseconds of the fault transient.

Cable and Converter Model

The cables are modeled using the Thévenin equivalent for the frequency dependent parameters model as described in Section 3.1.3 of Chapter 3. For those cables of which the propagation delay τ causes delays larger than the timeframe of interest, the voltage sources describing the waves reflected from remote terminals become short circuits.

For the converters, only the capacitive discharge stage is considered. Therefore, using the approach described in Section 3.2.4 of Chapter 3, the converters are modeled by an impedance Z^{conv}:

$$Z^{\mathrm{conv}} = R^{\mathrm{eq}} + sL^{\mathrm{eq}} + \frac{1}{sC^{\mathrm{eq}}}, \tag{6.9}$$

in which R^{eq}, L^{eq} and C^{eq} are the converter's equivalent resistance, inductance and capacitance, as given in (3.33)-(3.35) in Section 3.2.4 of Chapter 3.

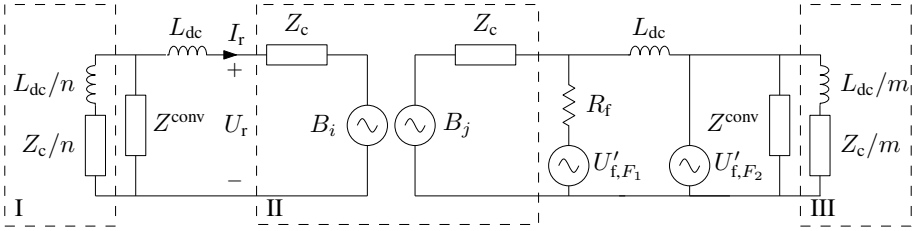


Figure 6.3: Reduced grid model to evaluate the transient waveforms resulting from faults at F_1 and F_2.

Grid Model

Fig. 6.3 shows the resulting reduced grid model to analyze the first incident wave for faults in a HVDC grid. The cable to be protected by the relay R (II) is terminated by inductors at each side, whereas the measurements I_r and U_r are at the cable side of the inductor. At each termination, a converter is modeled by its equivalent impedance Z^{conv}. The cables connected to the rest of the HVDC grid (I and III) are modeled by the characteristic impedance Z_c in series with an inductor L_{dc}. This assumes that traveling waves reflected by remote terminals do not impact u_r and i_r within the time frame of interest.

The cables are assumed to have the same characteristic impedance Z_c. Therefore, the n or m cables departing from the terminals adjacent to the faulted cable are modeled as one parallel equivalent branch (Fig. 6.3). It should be noted that, in case no other cables are connected at a termination (n or m equal to zero), parts I and III in Fig. 6.3 must be omitted.

In this form, the grid model is directly applicable for the analysis of pole-to-ground faults in an asymmetric monopolar system or bipolar system, considering solid grounding at each terminal. The analysis using this grid model can be extended to pole-to-pole faults in a symmetric monopolar system, considering appropriate adaptation of the pole-to-ground voltages and impedances to their pole-to-pole equivalents. To study different grounding schemes in asymmetric monopolar or bipolar systems, the grounding impedance and metallic return cable should be included in the model. These impedances would appear in series with the converter impedance.

Time Domain Response

As all components in the reduced grid model are linear, the model can be described in the Laplace domain. To obtain a time domain response, the

Table 6.1: Grid and converter parameters.

Dc voltage (pole-to-ground) U_{dc}	320 kV
Inductor L_{dc}	25 mH
Cable length l	200 km
Number of cables at bus n	2
Number of cables at bus m	2
C^{eq}	175.8 μF
L^{eq}	0.0383 mH
R^{eq}	0.295 Ω

transfer function of the voltage and current at the fault location to the relay location is first derived from the model (cf. Appendix D). Subsequently, a step input with magnitude $-U^0$ is used for U'_{f}, where U^0 is the pre-fault voltage. An approximation for the time domain solution was found by discretizing the transfer function using zero-order hold and solving the discretized system.

6.3.2 Determination of Thresholds

Fig. 6.4 shows the locus of the voltage and voltage derivative of u_{r} for pole-to-ground faults F_1 and F_2. In Fig. 6.4, the starting criterion and discrimination criteria based on the voltage are also plotted. This figure is obtained using the model depicted in Fig. 6.3 and the parameters enlisted in Table 6.1. The system configuration is asymmetric monopolar with pole-to-ground voltage 320 kV. The fault at F_1 has a resistance of 10 Ω and the fault at F_2 has a resistance of 0 Ω.

Fault Detection

The undervoltage threshold is used to discriminate faults from normal operation. The threshold can in theory be set to the minimal allowed voltage during normal operation. As an example, the undervoltage threshold was set to 85% of the nominal voltage (320 kV) in Fig. 6.4.

Fault Discrimination

For the discrimination stage, the thresholds for the voltage derivative and undervoltage criterion can in theory be set to the minimum values occurring for a solid fault at F_2 at $t = 0$, as shown in Fig. 6.4:

$$du^{\mathrm{thr},1} = \min_t \left(\frac{du_{\mathrm{r},F_2}}{dt} \right) \tag{6.10}$$

$$u^{\mathrm{thr},1} = u_{\mathrm{r},F_2}(t^{\mathrm{d}} + \Delta t^{\mathrm{discr}}), \tag{6.11}$$

in which u_{r,F_2} is the voltage measured at R for F_2. Fig. 6.4 visualizes these thresholds by showing the voltage-voltage derivative pairs as a function of time. The dot markers indicate samples taken at a sampling frequency of 100 kHz, starting from fault detection. The time $\Delta t^{\mathrm{discr}}$ for the undervoltage criterion has been taken as 100 μs, which corresponds to the tenth sample after fault detection, indicated by the square marker in 6.4.

A lower sampling frequency leads to a less sensitive protection algorithm. The algorithm makes use of the high frequency content of the voltage wave of internal faults to discriminate them from external ones. As shown in Section 5.4 of Chapter 5), lowering the sampling frequency leads to removal of high frequency content of the voltage wave.

6.3.3 Sensitivity Analysis

To demonstrate the validity of the protection algorithm, a sensitivity analysis is performed towards protection thresholds and sensitivity towards fault resistance. The considered parameters are series inductor value L_{dc}, grid topology at the bus where the relay R is located (by varying the number of cables n in Fig. 6.3) and cable length l.

The thresholds for the undervoltage and voltage derivative criterion are shown in Figs. 6.5 and 6.6 for various inductor values and grid topologies. For Figs. 6.5 and 6.6, the selected cable length is 200 km. To investigate the sensitivity of the protection algorithm, the maximum fault resistance for faults F_1 that can be discriminated from solid faults F_2 is plotted as function of inductor value and cable length in Fig. 6.7.

The undervoltage and voltage derivative thresholds $u^{\mathrm{thr},1}$ and $du^{\mathrm{thr},1}$ show a similar variation with L_{dc}, as the voltage derivative of u_{r} resulting from a solid fault at F_2 does not show a large variation within the interval $[t^{\mathrm{d}},t^{\mathrm{d}} + \Delta t^{\mathrm{discr}}]$ (Fig. 6.4).

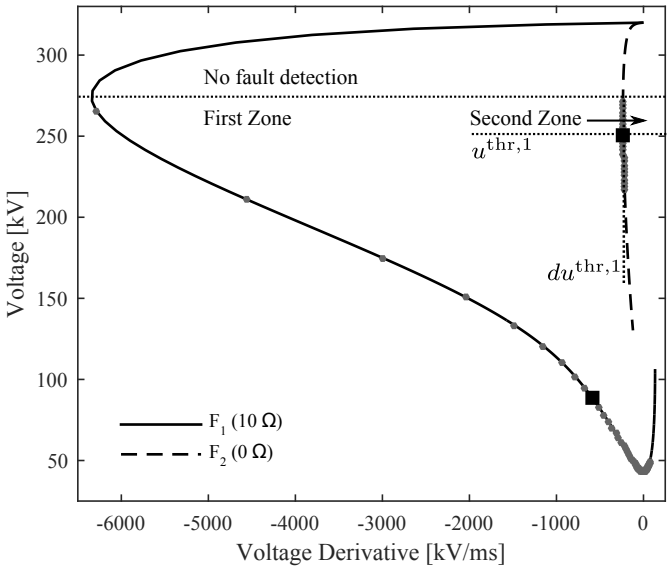


Figure 6.4: Protection zones and thresholds in the voltage/voltage derivative plane.

The variation of $u^{\mathrm{thr},1}$ and $du^{\mathrm{thr},1}$ decreases with increasing L_{dc}. This can be explained assuming a lossless line with a constant characteristic impedance Z'_{c} (cf. Section 6.1). In this case, the response of $U_{\mathrm{f},F_2}/U'_{\mathrm{f}}$ for a step input in U'_{f} is a first order response with time constant $L_{\mathrm{dc}}/Z'_{\mathrm{c}}$ (cf. (6.4)). Increasing L_{dc} thus causes a less steep wavefront for faults at F_2, allowing to set higher absolute values for $u^{\mathrm{thr},1}$ and $du^{\mathrm{thr},1}$. With increasing L_{dc}, the effect of the increasing time constant decreases within the time frame of fault detection and discrimination. In the frequency domain, this is reflected by the shift of the pole at $Z'_{\mathrm{c}}/L_{\mathrm{dc}}$ in (6.4). This pole shifts to the left at a decreasing rate as a function of L_{dc}.

The effect of grid topology is limited and decreases with increasing L_{dc}. With increasing L_{dc}, the current wave is increasingly suppressed during the interval $[t^{\mathrm{d}}, t^{\mathrm{d}} + \Delta t^{\mathrm{discr}}]$ (e.g., for a lossless cable with inductive termination, the time constant L_{dc}/Z'_{c} in (6.6) increases). Therefore, insensitivity towards variations in grid topology can be achieved using only the voltage measured at the terminals.

Discrimination of faults F_1 from a solid fault F_2 becomes more difficult for larger fault resistances of F_1. Increasing the fault resistance results in a decreased amplitude of U_{f,F_1} for all frequencies (cf. (6.3)). Consequently, the derivative

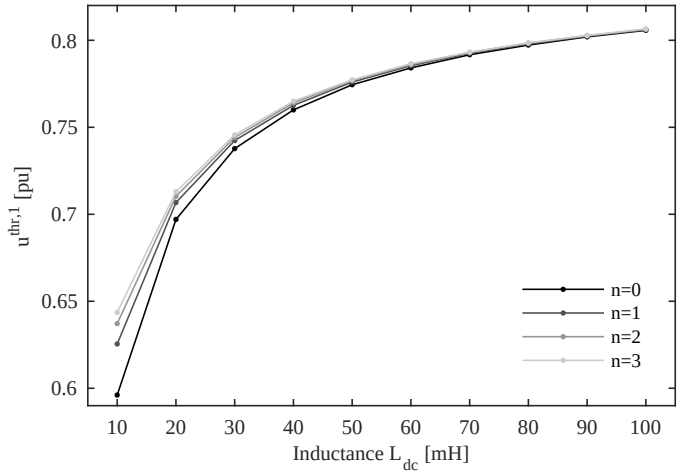


Figure 6.5: Voltage threshold in function of inductor value and grid topology (by varying number of cables n).

of u_r decreases and the decrease in voltage during the interval $[t^\mathrm{d}, t^\mathrm{d} + \Delta t^\mathrm{discr}]$ is lower, resulting in loci of the voltage/voltage derivative pairs closer to the thresholds defining the second zone (Fig. 6.4).

For a given cable length l, the maximum fault resistance for which faults F_1 and F_2 can be discriminated increases with L_dc. With increasing L_dc, the rate of change of u_r decreases since the time constant $L_\mathrm{dc}/Z'_\mathrm{c}$ increases. Consequently, a higher fault resistance for faults F_1 can be tolerated before F_1 and F_2 can no longer be discriminated.

The maximal fault resistance which allows fault discrimination decreases with increasing l (Fig. 6.7). The cable propagation function has a low-pass characteristic and passes through less high frequency content with increasing l (cf. Chapter 5). Therefore, with increasing l, the low-pass filtering of the wavefront resulting from faults at F_2 by L_dc relatively decreases with respect to the low-pass filtering by the cable propagation function H.

6.4 Case Study

In this section, the validity of the results obtained by the reduced grid model is demonstrated by a case study using a detailed test system implemented in

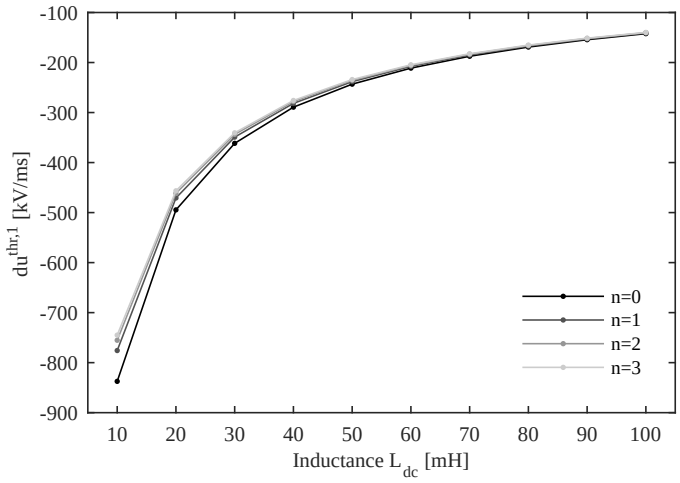


Figure 6.6: Voltage derivative threshold in function of inductor value and grid topology (by varying number of cables n).

PSCAD.

6.4.1 Test System

The test system for the case study is the four-terminal HVDC grid test system described in Appendix A and shown in Fig. 6.8. For this study, two values for L_{dc} were taken, i.e., 20 and 40 mH. The pre-fault power setpoints for the converters are those for the base case described in Table A.2 in Appendix A.

The faults studied in the test system are faults at F_1 and F_2, respectively occurring at the end of L_{13} and at bus 3 (Fig. 6.8). For both faults, the fault type is pole-to-pole with a connection to ground, where the fault resistance is divided equally between positive and negative pole.

For fault detection and discrimination for L_{13}, voltages and currents are measured at R_{13} and R_{31}. For the detailed model, the positive pole-to-ground quantities, e.g., voltage, current and fault resistance, are used. This enables a direct comparison of the results of the simulations of the detailed model against the reduced grid model with converter parameters given in Table 6.1. These equivalent converter parameters were calculated for the converters as described in Section 3.2.4 of Chapter 3 and transformed to parameters for the equivalent asymmetric system. The detailed test system was implemented in PSCAD and

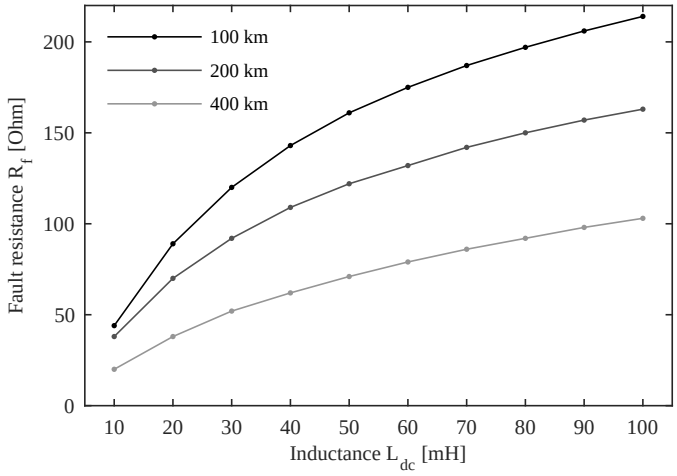


Figure 6.7: Maximal fault resistance in function of inductor value for different cable lengths l.

simulations were performed with a time step of 10 μs. For the reduced grid model, the transfer functions were first discretized with a time step of 0.5 μs, before the discretized system was solved to obtain a time domain response.

6.4.2 Comparison with Detailed Model

Fig. 6.9 shows the magnitude and voltage derivative of the voltage measured at R_{13} for faults F_1 and F_2 (with fault resistances of 60 and 0 Ω), as obtained by the reduced grid model and the benchmark model. Qualitatively, the waveforms obtained by both models correspond well. Table 6.2 shows a comparison of the thresholds predicted by the reduced model with the ones obtained by the benchmark model. The relative errors between thresholds obtained by both models do not exceed 0.5%, which confirms the suitability of the reduced model to determine protection thresholds. Table 6.2 further enlists the protection thresholds for both models for the 40 mH case. This case also demonstrates the suitability of the reduced model introduced in Section 6.3.1 to determine the protection thresholds, with relative errors below 0.2% compared to the detailed model.

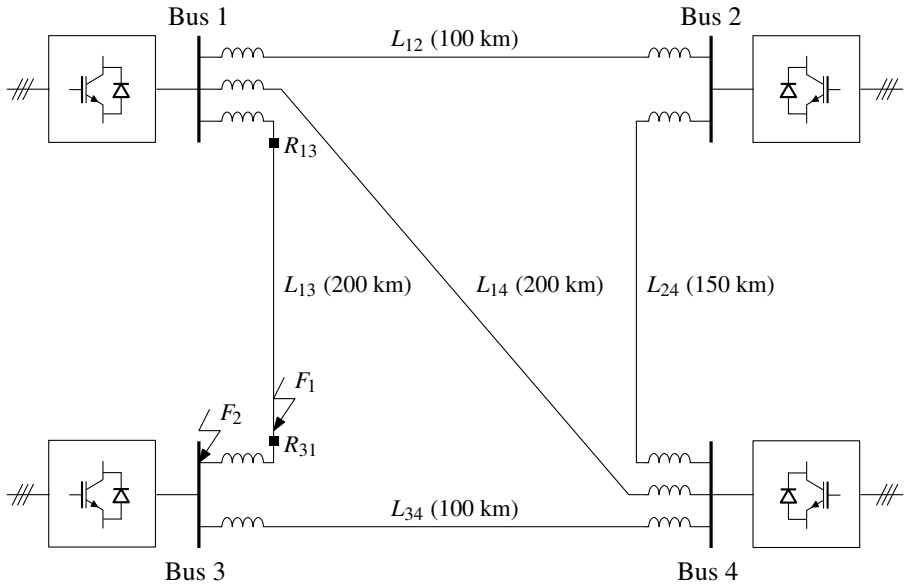


Figure 6.8: Four-terminal HVDC grid test system with relays R_{13} and R_{31} and faults F_1 and F_2.

Table 6.2: Thresholds for reduced grid model and benchmark model.

L_{dc}	Threshold	Red. Model	Benchmark Model	Rel. error
20 mH	$u^{\mathrm{thr},1}$ [pu]	0.7110	0.7110	0.0042%
	$du^{\mathrm{thr},1}$ [kV/ms]	-461.4483	-463.5521	0.4539%
40 mH	$u^{\mathrm{thr},1}$ [pu]	0.7640	0.7639	0.0160%
	$du^{\mathrm{thr},1}$ [kV/ms]	-278.0237	-278.4370	0.1485%

6.4.3 Time Domain Results

The proposed protection algorithm was implemented in PSCAD for testing with the detailed model. The results are shown for $L_{\mathrm{dc}} = 20$ mH. The faults F_1 and F_2 in Fig. 6.8 have a fault resistance of 60 and 0 Ω, respectively, and were initiated at $t = 2$ ms. The voltages and currents measured at R_{13} and R_{31} are denoted by u_{R13}, i_{R13}, u_{R31} and i_{R31}, respectively.

Fig. 6.10 shows all voltages and currents at relays R_{13} and R_{31} for F_1. At R_{31}, $t^{\mathrm{d}} = 0$ and a trip signal is sent to the associated breaker at $t = 2$ ms. After fault discrimination at $t = 2.1$ ms and due to the breaker delay of 2 ms, fault

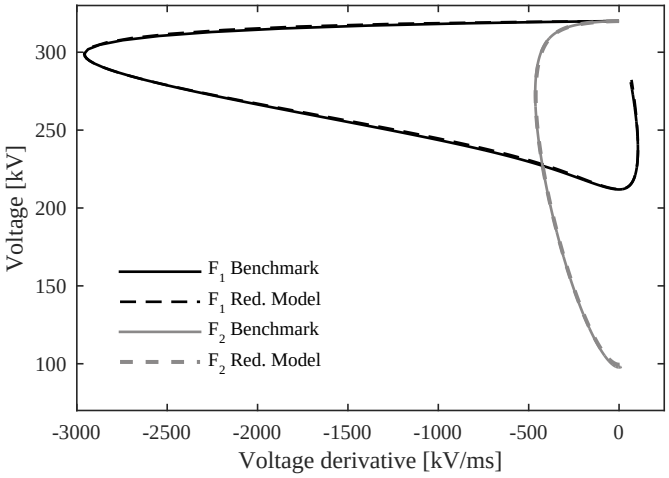


Figure 6.9: Comparison of magnitude and derivative of the voltage measured at R_{13} obtained with reduced grid and benchmark model for faults at F_1 (60 Ω) and F_2 (0 Ω).

Table 6.3: Output of fault detection and discrimination criteria.

	F_1 (60 Ω)			F_2 (0 Ω)		
Relay	$u^{\mathrm{thr},1}$	$du^{\mathrm{thr},1}$	Dir.	$u^{\mathrm{thr},1}$	$du^{\mathrm{thr},1}$	Dir.
R_{13}	1	1	1	0	0	1
R_{31}	1	1	1	1	1	0

current interruption at R_{31} starts at $t = 4$ ms. At $t = 4$ ms, u_{R31} increases and i_{R31} decreases due to insertion of the breaker surge arrester.

Due to wave propagation delay over the cable between converters 1 and 3, the traveling wave initiated by F_1 reaches R_{13} at $t = 3.09$ ms and is detected at $t^{\mathrm{d}} = 3.11$ ms. Consequently, after fault discrimination at $t^{\mathrm{d}} + \Delta t^{\mathrm{discr}}$ and with the breaker delay of 2 ms, fault current interruption at R_{13} starts at $t = 5.11$ ms.

For F_2, the protections that are triggered are shown in Table 6.3. At R_{13} a fault is detected in the forward direction but outside the first protection zone. For R_{31}, the directional criterion based on the current derivative inhibits tripping of the breaker.

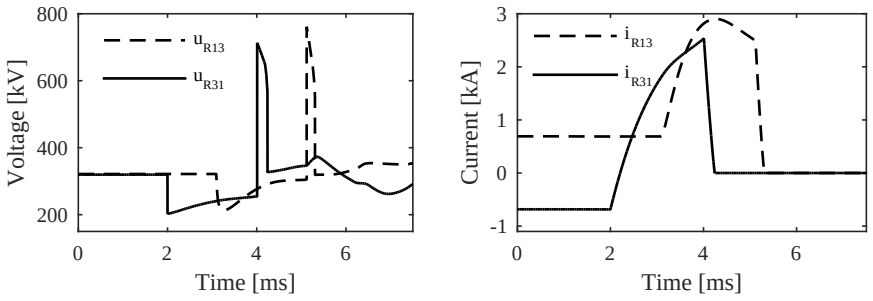


Figure 6.10: Positive pole-to-ground voltage (a) and currents (b) measured at R_{13} and R_{31} for a pole-to-pole fault at F_1 (60 Ω).

6.5 Conclusion

For a meshed HVDC cable grid with inductive termination, protection zones can be defined based on the inductive termination of the cables. The inductive termination largely reflects incident voltage waves created by faults on the cable to be protected and forms a low-pass filter for waves created by faults external to the cable. Exploiting this characteristic, a protection algorithm is proposed which uses the voltage magnitude and derivative of the first incident wave resulting from a fault to discriminate between internal and external faults in the forward direction of the relay. To identify faults in the backward direction of the relay, the current derivative is used. The thresholds for the protection algorithm can be efficiently determined with a reduced HVDC grid model which models only the faulted cable and its adjacent terminals.

A sensitivity analysis of the protection thresholds and sensitivity of the algorithm towards fault resistance demonstrates the validity of the proposed algorithm for a large range of parameters. First, the sensitivity of the protection thresholds to variations in the grid topology at the relay location is low and decreases with increasing series inductance. Second, the variation of the protection thresholds decreases with increasing series inductance. Third, the maximal fault resistance which allows the protection algorithm to discriminate between faults on the cable and faults external to the cable decreases with increasing cable length, but increases with increasing series inductance.

The comparison of thresholds obtained with the reduced model against thresholds obtained by simulation with a detailed model in EMT-type software justifies the use of the reduced model to determine protection thresholds. A case

study furthermore shows that the proposed protection algorithm can reliably detect and discriminate faults in the four-terminal HVDC grid test system of Appendix A.

Chapter 7

Backup Protection Algorithms for HVDC Grids

*The results of this chapter have been published as "W. Leterme, S. Pirooz Azad and D. Van Hertem, A local backup protection algorithm for HVDC grids, in IEEE Trans. Power Del., vol. 31, no. 4, pp. 1767-1755, Aug. 2016" and "S. Pirooz Azad, W. Leterme and D. Van Hertem, Fast breaker failure backup protection for HVDC grids, in Electric Power Systems Research Special Issue: Papers from the 11th International Conference on Power Systems Transients (IPST), vol. 138, pp. 99-105, Jun. 2016".**

Backup protection must be provided in case of primary protection failure, such as primary breaker or relay failure. For HVDC grids, the main constraint for backup protection is the high operation speed, as any delay in backup operations will result in increased required ratings for equipment such as dc breakers and HVDC converters. However, a delay between primary and backup protective actions is required to prevent backup prior to primary actions [148].

In the literature, algorithms for breaker failure were proposed in [28, 32, 149]. As mentioned in [149], traditional breaker failure detection which relies on overcurrent detection, results in considerable delays. During fault current interruption, the rate of decrease of the fault current is limited due to the series inductor and furthermore depends on fault location. Therefore, methods which

*The papers are mainly the result of joint research by the first two authors. The contributions of the first, respectively second, author are the development of the proposed backup protection principles for local and remote backup, the implementation of the backup protection algorithm employing the linear threshold and the simulations performed in the test system in PSCAD.

use overcurrent detection, as proposed in [28, 32] require a delay of at least the primary fault clearance time for the worst case scenario. The algorithm proposed in [149] tries to increase speed of breaker failure detection by making use of breaker internal measurements. Although this algorithm is fast, its dependence on breaker's internal measurements limits its application in multi-vendor HVDC grids.

In this chapter, relaying algorithms for HVDC grid backup protection to deal with breaker and relay failure are proposed. The main feature of the proposed algorithms is the resulting short delay between primary and backup protective actions, while providing enough time to the primary protection to initially clear faults. This is achieved through detecting uncleared faults shortly after initiation of fault current interruption by primary protection, rather than delaying uncleared fault detection until primary protection failure.

Section 7.1 first introduces current practice with respect to local and remote backup protection in ac systems. Thereafter Section 7.2 introduces the specific nature of the waveforms associated with breaker operation and fault clearing in HVDC grids, based on which the developed local backup protection algorithm for HVDC grids is presented. Section 7.2 furthermore highlights the difference between the proposed local backup protection algorithm for HVDC grids and those used in ac systems. Section 7.3 presents the proposed remote backup protection algorithm which deals with a different set of faults compared with the local algorithms. Next, in Section 7.4, the results of the application of the proposed algorithms to the four-terminal HVDC grid test system of Appendix A are presented. Finally, Section 7.5 presents the conclusions of this chapter.

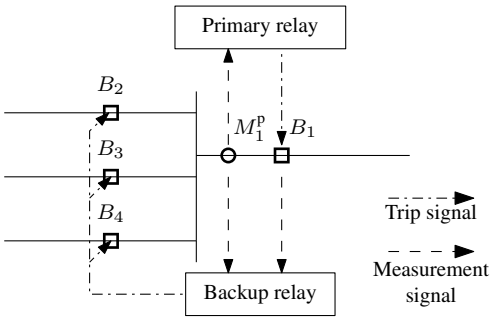
7.1 Backup Protection in Ac Systems

This section introduces the schemes used for backup protection in ac systems and presents the sequence of actions for fault clearing with primary and backup protection.

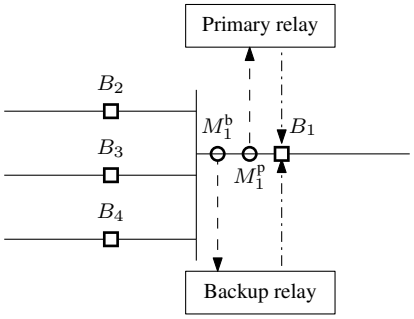
7.1.1 Local Backup Protection

Local Backup Protection

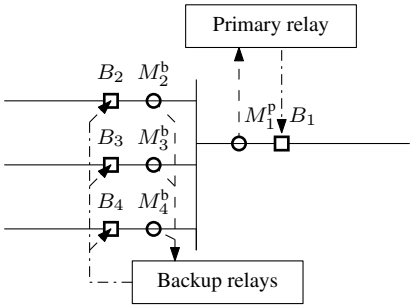
Fig. 7.1 presents an overview of possible backup protection schemes. It shows one backup protection scheme for breaker failure and two backup protection schemes in case of primary relay failure. In Fig. 7.1, the breaker associated with



(a) Backup protection for breaker failure.



(b) Backup protection for relay failure-duplication of the primary relay.



(c) Backup protection for relay failure-reverse reach.

Figure 7.1: Backup protection schemes for breaker failure (a) and relay failure (b), (c).

the primary relay is identified as B_1 and the adjacent breakers are B_2-B_4. The measurements (M_i) for the primary and backup protection are identified by superscript p and b, respectively.

Breaker Failure Backup Protection A breaker failure is identified if the current through the breaker associated with the primary relay exceeds a threshold after a certain time following fault detection by the primary relay. If the backup protection system detects a breaker failure, it will trip all adjacent breakers (Fig. 7.1 (a)).

Relay Failure Backup Protection Two backup protection schemes are proposed in the literature to deal with primary relay failures [150]: (i) duplication of the primary protection system and (ii) reverse reach. The primary relay might fail to detect faults due to the failure of measurement devices, communication system or the relaying algorithm itself [148].

In practice, it is possible to duplicate all protection equipment such as measurement devices and relays, except for the circuit breakers [150] (Fig. 7.1 (b)). To avoid common mode failure, the backup relay should use a different protection principle than the primary relay. The main advantage of this backup protection is its fast operation, since in this case no additional delay is needed, but this comes at the cost of additional measurement devices and relaying equipment.

For a backup scheme making use of reverse reach, adjacent relays provide local backup protection for the faulty relay by setting a reverse reach [88]. As an example, in ac systems, reverse reach can be provided by distance protection if one of the protection zones is set to detect faults in the backward direction of the relay [148]. The adjacent relays detect the fault independently of the primary relay and, in case of an undetected fault, trip all the breakers connected to the local bus (Fig. 7.1 (c)). This backup protection scheme does not require extra equipment, but is slower compared to duplication of the primary protection. Furthermore, for a single breaker scheme as shown in Fig. 7.1 (c), the entire bus is lost in case of an undetected fault on any of the connected lines.

Local Backup Protection Actions

In ac systems, the fault clearance time in case of primary protection failure is the sum of the primary fault clearance time, a delay between primary and backup actions and the backup protection fault clearance time. Fig. 7.2, adapted from [148], shows the time continuum of primary and backup protection actions

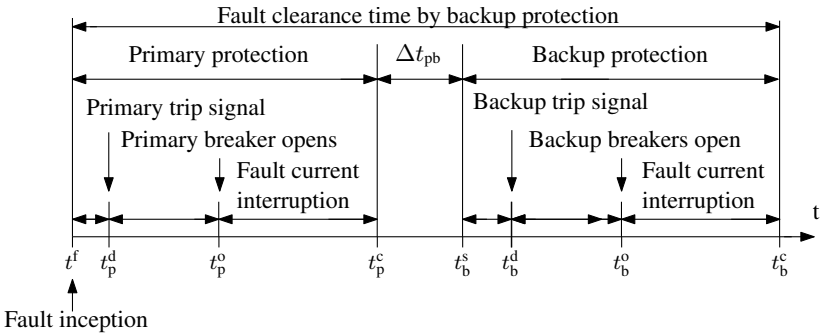


Figure 7.2: Primary and backup protection continua in ac systems.

in ac systems, as could be used for a breaker or relay failure scheme shown in Figs. 7.1a and 7.1c, respectively.

The primary protection system detects the fault at $t_{\mathrm{p}}^{\mathrm{d}}$, which is the sum of t^{f}, i.e., the time required for the fault wave to reach the relay, processing time to detect the fault, and time to send a trip signal to the associated breaker. The associated breaker opens at $t_{\mathrm{p}}^{\mathrm{o}}$ and interrupts the fault current at $t_{\mathrm{p}}^{\mathrm{c}}$. The backup protection initiates detection of primary protection failure at $t_{\mathrm{b}}^{\mathrm{s}}$, which is the sum of $t_{\mathrm{p}}^{\mathrm{c}}$ and a delay Δt_{pb}. If primary protection failure is detected at $t_{\mathrm{b}}^{\mathrm{d}}$, the backup protection trips the breakers on all lines adjacent to the faulted line. The adjacent breakers open at $t_{\mathrm{b}}^{\mathrm{o}}$ and interrupt the fault current at $t_{\mathrm{b}}^{\mathrm{c}}$. The total time required to clear the fault in case of primary protection failure is $t_{\mathrm{b}}^{\mathrm{c}} - t^{\mathrm{f}}$.

In ac backup protection, Δt_{pb} typically takes a value of multiple cycles of the fundamental frequency [150] to avoid tripping of multiple circuit breakers due to misoperation of the backup protection. For HVDC grid protection, such a large margin would lead to impractical requirements on ratings of dc breakers and HVDC converters, since these would be subjected to high currents and low voltages for an extensive period of time.

7.1.2 Remote Backup Protection

Remote backup protection in ac systems must be provided in case the fault cannot be cleared solely by local backup protection actions [148]. The ability of the local backup protection to clear the fault mainly depends on the switching station arrangement. For a single-line/single-breaker station arrangement, in case of breaker failure, the local backup protection is able to completely clear

faults on lines, whereas faults on a bus require tripping of the remote breaker. For a ring bus or breaker-and-a-half station arrangement, in case of breaker failure, the breakers associated with local backup protection cannot completely clear the fault and must be assisted by breakers at remote stations [150]. Consequently, for a single-line/single-breaker arrangement, backup protection is needed only for faults on a remote bus. By contrast, for a ring bus or breaker-and-a-half station arrangement, backup protection is needed for faults on a remote bus or remote lines.

Remote backup protection in ac systems can be provided by overcurrent or distance relays with an intentional time delay to avoid backup operation prior to the primary and local backup protection. To coordinate the remote backup protection with the primary and local backup protection, e.g. for distance protection, actions for faults in different protection zones are coordinated with time intervals which allow the previous zone to clear the fault first [89]. The coordinating time intervals are in the order of hundreds of milliseconds. Similar to local backup protection, the use of such large margins in HVDC grid protection would result in impractical requirements on ratings of dc breakers or converters.

7.2 HVDC Grid Local Backup Protection

In this section, the local backup protection algorithm is proposed and compared with the current practice in ac systems. The proposed local backup protection algorithm consists of two separate subsystems which detect (i) failure of the breaker associated with the primary relay (Fig. 7.1a) and (ii) failure of relays on adjacent lines (Fig. 7.1c).

First, the actions taken by the backup protection in function of time are presented in Section 7.2.1. Second, the waveforms specific to fault clearing by primary and backup protection in HVDC grids are described in Section 7.2.2. Third, two implementations of the proposed local backup protection algorithm for HVDC grids, which exploits the particular nature of these waveforms, are presented.

7.2.1 Proposed Backup Protection Principles

The proposed local backup protection algorithm achieves a high operation speed by detecting primary protection failure shortly after the instant at which the primary protection is expected to initiate fault current interruption, i.e.,

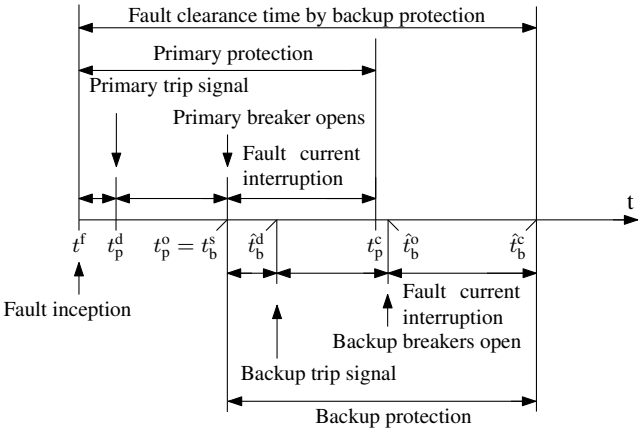


Figure 7.3: Primary and proposed local backup protection continua in HVDC grids.

$t_{\mathrm{p}}^{\mathrm{o}}$ (Fig. 7.3). In Fig. 7.3, similar to Fig. 7.4, t^{f}, $t_{\mathrm{p}}^{\mathrm{d}}$ and $t_{\mathrm{p}}^{\mathrm{o}}$ correspond to the fault inception, fault detection and expected primary fault current interruption initation instants. From $t_{\mathrm{p}}^{\mathrm{o}}$, the local backup protection algorithm starts tracking uncleared faults. If the primary protection succeeds in interrupting the fault current, the backup protection algorithm detects a cleared fault and no backup protective actions are carried out. If the primary protection fails, the backup protection algorithm detects an uncleared fault at $\hat{t}_{\mathrm{b}}^{\mathrm{d}}$ and trips the adjacent breakers to interrupt the fault current. The adjacent breakers open at $\hat{t}_{\mathrm{b}}^{\mathrm{o}}$ and the backup protection clears the fault at $\hat{t}_{\mathrm{b}}^{\mathrm{c}}$.

Compared to algorithms based on the philosophy shown in Fig. 7.2, algorithms based on the proposed principles pose less stringent requirements on ratings of HVDC grid components as the fault clearance time, and hence the system's exposure to low dc voltages and high currents, is shorter ($\hat{t}_b^c < t_b^c$). A comparison between Figs. 7.2 and 7.3 shows that the difference between t_b^c and $\hat{t}_b^c$ is the sum of the fault current interruption time by the primary protection ($t_p^c - t_p^o$) and the time delay between primary and backup protective actions Δt_{pb}, i.e., $t_p^c - t_p^o + \Delta t_{pb}$.

7.2.2 Loci of Dc Fault Currents and Voltages with Primary and/or Backup Protection in Service

A dc fault in a HVDC grid, in the initial stage, can be characterized by an increasing current and a decreasing voltage in the faulted pole. In case of

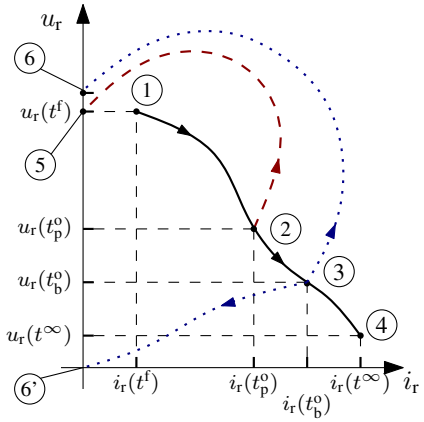


Figure 7.4: Conceptual overview of loci of the dc fault currents and voltages at the primary or adjacent relay for a cleared and an uncleared fault.

pole-to-ground faults in a high impedance grounded system, the fault current in the faulted pole oscillates and returns to zero. In case of a pole-to-ground fault in a low impedance grounded system or pole-to-pole fault, the current increases to a high prospective steady-state value.

Fig. 7.4 provides a conceptual overview of the loci of the dc voltage and current for a cleared and an uncleared fault as a function of time (assuming a high prospective steady-state fault current). The voltage and current are measured between the dc breaker and inductor, considering the breaker is located at the cable end. To simplify Fig. 7.4, oscillations caused by traveling wave reflections were excluded. The actual shape of the curve does not correspond to a certain typical fault current development, but merely reflects its general non-linear nature. In Fig. 7.4, points 1 and 2 correspond to fault inception and breaker opening instants, t^{f} and $t_{\mathrm{p}}^{\mathrm{o}}$, respectively. The solid line from point 1 to point 2 shows the variations in the current and voltage measured at the primary relay during the $[t^{\mathrm{f}}\ t_{\mathrm{p}}^{\mathrm{o}}]$ interval as the fault is detected by the primary protection system and the primary breaker trip signal is generated. The dashed line between points 2 and 5 shows the loci of dc voltages and currents after the primary breaker trips and the faulty line is removed. As the fault is being cleared, the voltage increases from $u_{\mathrm{r}}(t_{\mathrm{p}}^{\mathrm{o}})$ to $u_{\mathrm{r}}(t^{\mathrm{f}})$ and the current decreases from $i_{\mathrm{r}}(t_{\mathrm{p}}^{\mathrm{o}})$ to 0. To ensure safe post-fault operation, control actions subsequent to the protective actions might be required to alter this voltage.

In Fig. 7.4, the solid line from point 2 to point 4 shows the loci of dc voltages and currents measured at the primary relay after primary protection failure. For an uncleared fault, the voltage decreases from $u_{\mathrm{r}}(t_{\mathrm{p}}^{\mathrm{o}})$ to $u_{\mathrm{r}}(t^{\infty})$ and the

current increases until a steady-state value, $i_{\mathrm{r}}(t^{\infty})$, is reached at point 4.

If the backup protection clears the fault after primary protection failure, the dc voltages and currents will follow the path from point 2 to point 3 and then to point 6 (in case of relay failure) or 6' (in case of breaker failure). The actual voltage at point 6 depends on the response of the protection associated with the converter. Fig. 7.4 shows a possible example, in which the converter located at the bus is assumed to remain connected at the bus, thereby supporting the recovering dc voltage.

Based on the backup protection algorithm, the backup protective actions begin at $t_{\mathrm{b}}^{\mathrm{o}}$ and continue through the $[t_{\mathrm{p}}^{\mathrm{o}}, t_{\mathrm{b}}^{\mathrm{c}}]$ interval. During the $[t_{\mathrm{p}}^{\mathrm{o}}, t_{\mathrm{b}}^{\mathrm{o}}]$ interval (from point 2 to 3) the current increases from $i_{\mathrm{r}}(t_{\mathrm{p}}^{\mathrm{o}})$ to $i_{\mathrm{r}}(t_{\mathrm{b}}^{\mathrm{o}})$. If the backup protection does not operate fast enough, $i_{\mathrm{r}}(t_{\mathrm{b}}^{\mathrm{o}})$ will exceed the current interruption capability of dc breakers and the fault cannot be cleared. The dotted line from point 3 to point 6, shows i_{r} and u_{r} as all transmission lines connected to the same bus as the faulty line are disconnected to clear the fault. At point 6 ($t_{\mathrm{b}}^{\mathrm{c}}$), the backup protection clears the fault and the dc fault current becomes zero.

7.2.3 Proposed Backup Protection Algorithms

Breaker failure detection using a linear threshold

In this approach, linear discriminant analysis (LDA) is used to find a threshold (or decision boundary) which divides the UI-plane of Fig. 7.4 into two regions associated with cleared and uncleared faults. LDA is a method that projects a set of samples, containing multiple features, into the direction which maximizes the separability among them [151]. The projection of each sample into this direction results in a transformed sample with a lower feature dimension in the new coordinate.

For the breaker failure relay, each sample x consists of two features (i^n, u^n), which are the instantaneous current and voltage measured at the primary relay of the line for which the breaker failure protection algorithm is designed. These samples are obtained by applying a number of faults along their associated line while the primary breaker is either enabled or disabled. Within the time interval $[t_{\mathrm{p}}^{\mathrm{o}}, \hat{t}_{\mathrm{b}}^{\mathrm{d}}]$, the voltage and current measurements at the primary relay are sampled at instants $t_n = t_{\mathrm{o}} + n\Delta t$ where Δt is a fixed time step. The obtained samples are divided into two sets, X_1 and X_2, which are defined as the sets of

samples associated with uncleared and cleared fault scenarios:

$$X_1 = \left\{ (i_{\mathrm{uc}}^1, u_{\mathrm{uc}}^1), (i_{\mathrm{uc}}^2, u_{\mathrm{uc}}^2), ..., (i_{\mathrm{uc}}^N, u_{\mathrm{uc}}^N) \right\},$$

$$X_2 = \left\{ (i_{\mathrm{c}}^1, u_{\mathrm{c}}^1), (i_{\mathrm{c}}^2, u_{\mathrm{c}}^2), ..., (i_{\mathrm{c}}^N, u_{\mathrm{c}}^N) \right\},$$

where N is chosen as $(t_{\mathrm{p}}^{\mathrm{o}} + N\Delta t) \leq \hat{t}_{\mathrm{b}}^{\mathrm{d}}$. An additional margin can be used to increase robustness of the breaker failure detection in case of uncertainty on $\hat{t}_{\mathrm{b}}^{\mathrm{d}}$.

For both sets, a matrix $\boldsymbol{S}_{\mathrm{i}}$ is defined as

$$\boldsymbol{S}_{\mathrm{i}} = \sum_{x \in X_{\mathrm{i}}} (x - \overline{x}_{\mathrm{i}})(x - \overline{x}_{\mathrm{i}})^{\mathrm{T}}, \tag{7.1}$$

where $\overline{x}_{\mathrm{i}}$ is the mean of X_{i}. The projection matrix w^* which maximizes the separability between samples of the two sets is

$$w^* = \boldsymbol{S}_{\mathrm{W}}^{-1}(\overline{x}_1 - \overline{x}_2), \tag{7.2}$$

where $\boldsymbol{S}_{\mathrm{W}}$ is the sum of $\boldsymbol{S}_1$ and $\boldsymbol{S}_2$. Using w^*, the projection of samples x_i from X_1 and X_2 results in two new sets Y_1 and Y_2 with one-dimensional samples y_i, where

$$y_i = (w^*)^{\mathrm{T}} x_i. \tag{7.3}$$

Cleared and uncleared faults are distinguished by comparing these projected samples to a threshold y^{thr}, which is defined as

$$y^{\mathrm{thr}} = \frac{y_1^{\mathrm{d}} + y_2^{\mathrm{d}}}{2}, \tag{7.4}$$

where y_1^{d} and y_2^{d} are the closest samples from Y_1 and Y_2, respectively.

Breaker and relay failure detection using classifiers

In this approach, the K nearest neighbor (KNN) classifier is used, as it provides a simple yet effective classification method [152]. A KNN classifier identifies the class of the unseen sample as the class majority of the k nearest neighbors. A nearest neighbor is defined as the sample from the training set that has the minimal distance to the unseen sample. The distance metric used is the Euclidean distance. The parameter k is a design parameter of the classifier and can be optimized based on the training samples.

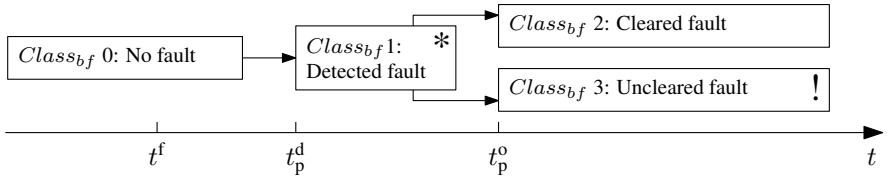


Figure 7.5: Classifier outputs for breaker failure detection (*: alert state, !: action state).

Breaker Failure Detection The classifier associated with the breaker failure subsystem uses three features from the current and voltage measurements at the primary protection zone; the instantaneous voltage and current and a time tag. To eliminate the impact of the pre-fault operating conditions, the pre-fault currents and voltages are subtracted from the instantaneous quantities. The time tag is used to separate the samples taken before $t_{\mathrm{p}}^{\mathrm{d}}$, during the $[t_{\mathrm{p}}^{\mathrm{d}}\ t_{\mathrm{p}}^{\mathrm{o}}]$ interval, and after $t_{\mathrm{p}}^{\mathrm{o}}$ and can take three values. The time tags of the training data are known and the default time tag of the test samples is 0.

The breaker failure classifier identifies whether the primary breaker operated or the fault remains uncleared although it was detected by the primary relay. This classifier assigns a class number to each unseen data sample (Fig. 7.5):

- *$Class_{bf}$ 0:* no fault is detected in the primary protection zone,
- *$Class_{bf}$ 1:* fault is detected in the primary protection zone, but fault current is not interrupted by the primary breaker yet,
- *$Class_{bf}$ 2:* the primary breaker operated and fault will be cleared, and
- *$Class_{bf}$ 3:* the primary breaker failed to remove the faulty line.

Classes 1 and 3 indicate the alert and action states, respectively. In the alert state, backup actions are delayed until a decision on primary protection failure is made. In the action state, a trip signal is sent to all adjacent breakers. Classes 0 and 2 indicate that no action from the breaker failure backup protection is required.

Relay Failure Detection The classifier associated with the relay failure subsystem is used to detect uncleared faults in the reverse backup protection zone of the relay. Such an uncleared fault is due to the failure of an adjacent relay for which the fault is in the primary protection zone.

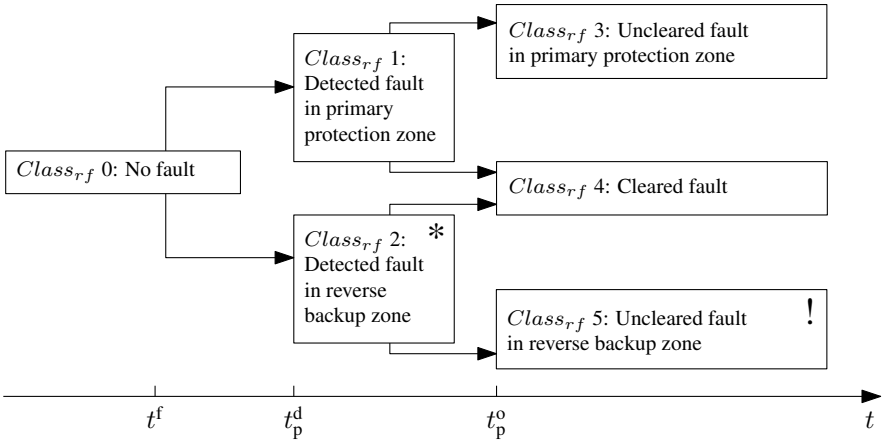


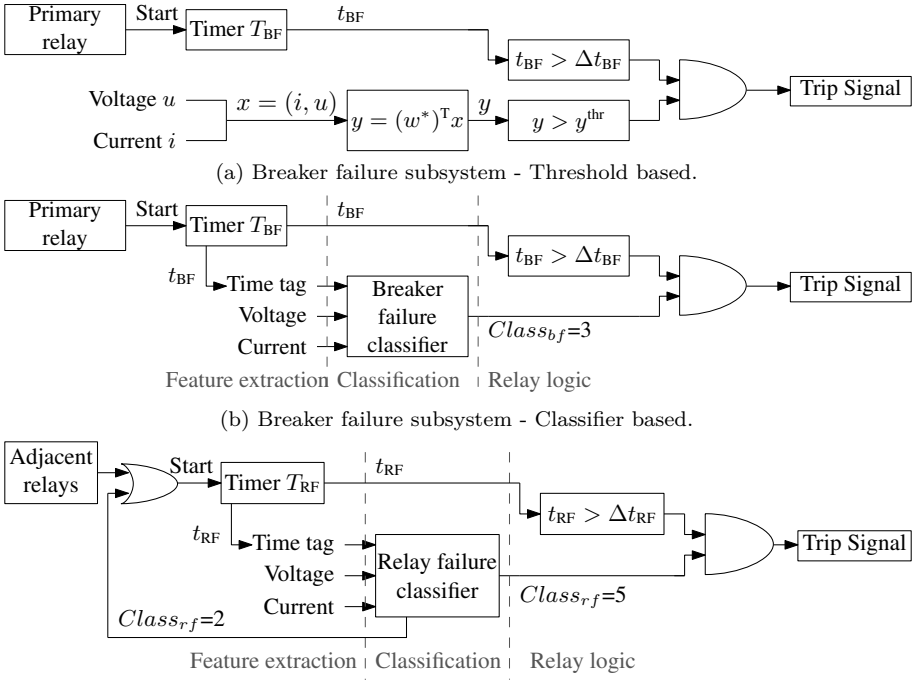
Figure 7.6: Classifier outputs for relay failure detection (*: alert state, !: action state).

The inputs to the relay failure classifier are the instantaneous current and voltage measurements and a time tag. The time tag determines the relative instant of the data sample with respect to the fault detection instant and takes similar values to that of the breaker failure classifier.

The output of each classifier can obtain 6 values (Fig. 7.6):

- *$Class_{rf}$ 0*: no fault is detected,
- *$Class_{rf}$ 1*: fault is detected in the primary protection zone,
- *$Class_{rf}$ 2*: fault is detected in the reverse backup protection zone,
- *$Class_{rf}$ 3*: fault in the primary protection zone is not cleared,
- *$Class_{rf}$ 4*: fault is cleared, and
- *$Class_{rf}$ 5*: fault in the reverse backup protection zone is not cleared.

Classes 2 and 5 indicate the alert and action states, respectively. Classes 0, 1, 3 and 4 do not require any protective action from the relay failure backup protection.



(a) Breaker failure subsystem - Threshold based.

(b) Breaker failure subsystem - Classifier based.

(c) Relay failure subsystem - Classifier based.

Figure 7.7: Block diagram of proposed backup protection system.

7.2.4 Summary

Fig. 7.7 summarizes the backup protection algorithm steps and the inputs and outputs of the backup protection system.

These steps are

- feature extraction: For the threshold-based approach, two features, i.e., instantaneous voltage and current are used. In the classifier-based approach, three features, i.e., time tag, instantaneous voltage and current, are extracted from the measurements and at each sampling instant provided to the subsystems. The time tags for the breaker and relay failure subsystems are generated by timers T_{BF} and T_{RF} which are activated through fault detection by (i) the primary relay for the breaker failure subsystem or (ii) the adjacent relays or the relay failure classifier, respectively. The relay failure classifier detects a fault in the reverse backup zone if the class number becomes 2.

- classification: For the threshold-based approach, the voltage and current samples are transformed to y. In the classifier-based approach, the classifier associated with each subsystem assigns a class number to the data sample.
- relay logic: For the threshold-based approach, in case $y > y^{\text{thr}}$ and t_{BF} exceeds Δt_{BF}, a trip signal is generated. In the classifier-based approach, the breaker failure and relay failure subsystem generate a trip signal if the class number is 3 or 5 and t_{BF} or t_{RF} exceed a threshold, Δt_{BF} or Δt_{RF}, respectively. The breaker failure trip signal is sent to the breakers on all lines adjacent to the faulted one. The relay failure trip signal is sent to the breakers on the adjacent lines and the breaker on the faulted line.

The thresholds Δt_{BF} and Δt_{RF} are used to ensure operation of the backup protection after the primary protection by controlling the time instants, $\hat{t}_{\text{b}}^{\text{d}}\{\text{BF}\}$ and $\hat{t}_{\text{b}}^{\text{d}}\{\text{RF}\}$, at which the backup protection starts to interrupt the fault current. The minimum value for Δt_{BF} in the breaker failure subsystem is the primary breaker opening time, i.e., $t_{\text{p}}^{\text{o}} - t_{\text{p}}^{\text{d}}$. In the relay failure subsystem, Δt_{RF} is equal to the sum of the primary relay detection time ($t_{\text{p}}^{\text{d}} - t^{\text{f}}$), breaker opening time, ($t_{\text{p}}^{\text{o}} - t_{\text{p}}^{\text{d}}$) and a safety margin to account for the uncertainties on the instant of fault detection by the adjacent relays or the relay failure classifier.

To ensure operation of the breaker failure subsystem prior to the relay failure subsystem, the thresholds Δt_{BF} and Δt_{RF} can be set such that $\hat{t}_{\text{b}}^{\text{d}}\{\text{RF}\} > \hat{t}_{\text{b}}^{\text{d}}\{\text{BF}\}$. The reason for this constraint is that the breaker failure subsystem is more robust than the relay failure subsystem, as the latter detects faults in the reverse backup protection zone whereas the former detects faults in the primary protection zone.

7.3 HVDC Grid Remote Backup Protection

Unlike the local backup protection algorithm, the proposed remote breaker failure backup protection algorithm deals with faults on remote buses in the forward direction of the relay. A fault in the forward direction can be in the relay primary protection zone, e.g., the line where the relay is located, or outside this zone, e.g., a remote bus or a remote line. For a remote bus fault, the relay must provide remote backup protection in case the breaker associated with the bus primary protection fails. Remote backup protection for line faults is not considered in this work as primary or local backup protection are required to clear those faults.

The remote breaker failure backup protection algorithm uses voltage and current measurements to detect and identify uncleared bus faults in the forward direction of the relay.

The remote backup protection algorithm must (i) detect faults, (ii) identify faults at remote buses and (iii) distinguish between bus faults cleared by the primary protection and uncleared ones. To achieve these objectives, the proposed backup protection algorithm operates in three steps.

First, the protection algorithm detects a fault in the forward direction if

$$\begin{aligned} u_{\mathrm{r}} &< u^{\mathrm{thr,d}} \text{ and} \\ i'_{\mathrm{r}} &> 0, \end{aligned} \tag{7.5}$$

where u_{r} and i_{r} are the voltage and transient component of the current measured at the relay and $u^{\mathrm{thr,d}}$ is a threshold on the voltage. The time instant at which (7.5) is satisfied, is denoted with $t^{\mathrm{d}}_{\mathrm{p}}$. If after $t^{\mathrm{d}}_{\mathrm{p}}$, the primary protection system associated with the relay detects a fault in its primary protection zone, a trip signal is immediately sent to the primary breaker. If the primary protection system detects a fault outside its zone, the backup protection algorithm will continue to operate.

Second, the protection algorithm discriminates between faults at remote buses from those at remote lines. To identify a fault at a remote bus, at time instant $t^{\mathrm{id}}_{\mathrm{rb}} = t^{\mathrm{d}}_{\mathrm{p}} + \Delta t^{\mathrm{id}}$, u_{r} and i_{r} are compared against thresholds $u^{\mathrm{thr,id}}$ and $i^{\mathrm{thr,id}}$:

$$\begin{aligned} u_{\mathrm{r}} &< u^{\mathrm{thr,id}}, \\ i_{\mathrm{r}} &> i^{\mathrm{thr,id}}. \end{aligned} \tag{7.6}$$

If (7.6) is not satisfied, the protection algorithm will detect a fault at a remote line and will not generate any trip signals.

The thresholds $u^{\mathrm{thr,id}}$ and $i^{\mathrm{thr,id}}$ allow the protection algorithm to discriminate between faults at remote lines and remote buses. Traveling waves created by faults at a remote line encounter an additional series inductor in their path (from the fault location to the relay), compared to those created by a remote bus fault. Therefore, when the former waves reach the relay, their wavefront is less steep than that of the latter.

Third, the protection algorithm detects an uncleared bus fault if, at time instant $t^{\mathrm{uc}}_{\mathrm{rb}} = t^{\mathrm{d}}_{\mathrm{p}} + \Delta t^{\mathrm{uc}}$,

$$u_{\mathrm{r}} < u^{\mathrm{thr,uc}}, \tag{7.7}$$

where $u^{\mathrm{thr,uc}}$ is a threshold. The remote backup protection algorithm will generate a trip signal if (7.7) is fulfilled. If (7.7) is not satisfied, no trip signal

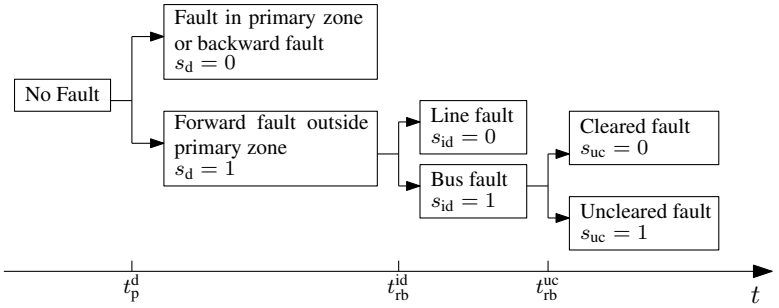


Figure 7.8: Decisions made by the remote backup protection algorithm as a function of time.

will be generated. In (7.7), only a voltage-based criterion is used to discriminate between cleared and uncleared faults as this selection minimizes the required time to detect uncleared faults. Due to the voltage inserted by the breaker surge arrester, the voltage for cleared faults takes values which clearly differ in magnitude from uncleared faults. Consequently, the voltage magnitude can be used to detect the persistence of a fault in the system.

A timer is used to control $t_{\mathrm{rb}}^{\mathrm{id}}$ and $t_{\mathrm{rb}}^{\mathrm{uc}}$ with respect to $t_{\mathrm{p}}^{\mathrm{d}}$. To distinguish cleared bus faults from uncleared ones, the delay between $t_{\mathrm{p}}^{\mathrm{d}}$ and $t_{\mathrm{rb}}^{\mathrm{uc}}$, Δt^{uc}, must be larger than the breaker opening time Δt^{o}. Since the measured voltage for a cleared bus fault increases after t^{o}, it becomes increasingly complex to distinguish cleared bus faults from remote line faults in case $t_{\mathrm{rb}}^{\mathrm{id}} - t_{\mathrm{p}}^{\mathrm{d}} > \Delta t^{\mathrm{o}}$. Consequently, to discriminate between remote line faults and bus faults, the delay between $t_{\mathrm{rb}}^{\mathrm{id}}$ and $t_{\mathrm{p}}^{\mathrm{d}}$, Δt^{id}, is preferably less than Δt^{o}.

Fig. 7.8 summarizes the steps and associated internal signals of the remote backup protection algorithm as a function of time. The true value of flag signals s_d, s_i and s_u corresponds to fault detection outside the primary protection zone, remote bus fault detection and uncleared fault detection, respectively. If (7.5), (7.6) and (7.7) are fulfilled at $t_{\mathrm{p}}^{\mathrm{d}}$, $t_{\mathrm{rb}}^{\mathrm{id}}$ and $t_{\mathrm{rb}}^{\mathrm{uc}}$, respectively, the internal signals will become 1. If all flag signals are 1 at $t_{\mathrm{rb}}^{\mathrm{uc}}$, the remote backup protection algorithm will generate a trip signal for its associated breaker.

7.4 Case Studies

The algorithms are tested in the four-terminal meshed test system described in Appendix A (Fig. 7.10). The series inductors are considered to be 50 mH. The

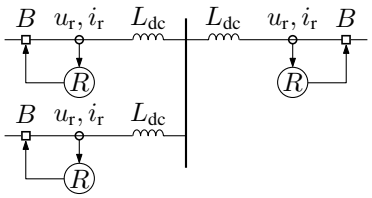


Figure 7.9: Single busbar layout with three infeeds, each with an inductor, a primary relay, a breaker and current and voltage sensors.

pre-fault settings for the converter powers are given in Table A.2 in Appendix A.

Fig. 7.9 shows the busbar layout and location of measurements considered in this study. Hybrid dc breakers with bidirectional current interruption capability are inserted at the end of each dc transmission line and at the converter's dc terminals. The pole-to-ground voltage and pole current measurements are assumed to be available at the line end of each inductor. The sign of the current is positive (negative) if the current flows in the direction of the transmission line (bus). The primary protection algorithm detects faults shortly after fault inception using an undervoltage criterion and is set to identify faults in the primary protection zone 0.3 ms later. The primary protection zone for each relay encompasses the entire transmission line for which the relay provides protection. The results are shown for pole-to-pole faults on the dc side. The breakers are opened 2 ms after fault detection, which can be achieved by pro-active breakers with an opening time of 2 ms or breakers without pro-active function with an opening time of 1.7 ms (cf. Section 2.1.3 of Chapter 2).

The results for the local backup protection algorithms associated with failure of B_{13} and R_{13} are discussed below. For the breaker failure backup protection for failure of B_{13}, measurements at R_{13} are used. The relay failure backup protection for relay failure of R_{13} uses measurements at R_{12} and R_{14}. The remote backup protection algorithm provides backup for breaker failure of B_{13} and uses measurements at R_{31}. The sampling time for voltage and current measurements is 0.02 ms, corresponding to a sampling frequency of 50 kHz. The simulation software used for the studies is PSCAD [102].

7.4.1 Breaker Failure Detection

The procedure for determining the threshold or training the classifier for the breaker failure subsystems is discussed first. Thereafter, for each subsystem, breaker failure detection of B_{13} is demonstrated for a fault in the middle of L_{13}

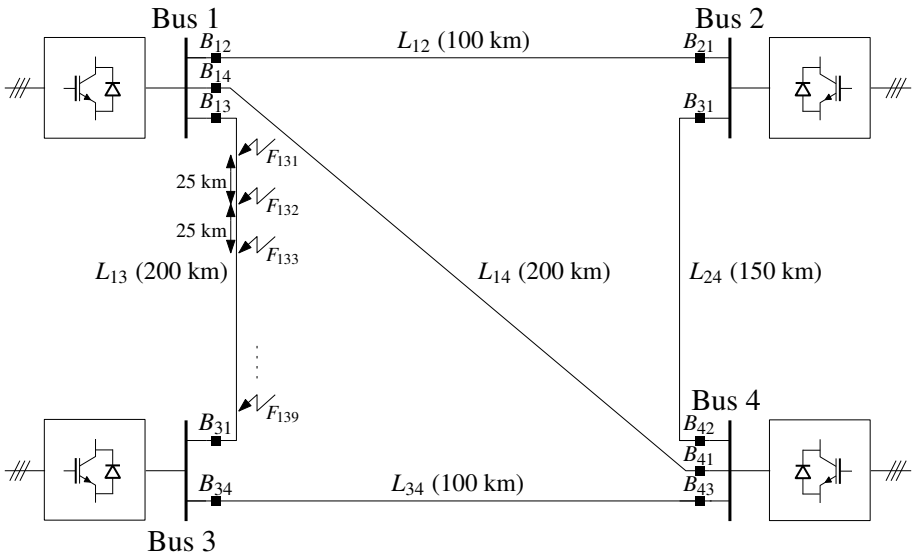


Figure 7.10: HVDC grid test system with faults and breakers.

for two scenarios. In scenario (i), the primary protection clears the fault and in scenario (ii), breaker B_{13} fails to interrupt the fault.

Linear Threshold

To determine the threshold for breaker failure of B_{13}, nine pole-to-pole faults were applied at equally-spaced distances on L_{13} of the test system of Fig. 7.10. Fig. 7.11 shows samples, taken at 200 μs-intervals within $[t_{\mathrm{p}}^{\mathrm{o}}$+0.2ms,$t_{\mathrm{p}}^{\mathrm{o}}$+1.2ms], on the loci of voltage and current for all faults and the threshold for breaker failure detection as proposed in 7.2.3.

With the threshold, the samples associated with cleared and uncleared faults can be discriminated irrespective of the time instant at which the backup protection is expected to operate (Fig. 7.11). The threshold is determined for the samples of Fig. 7.11 with the procedure described in Section 7.2.3. The interval Δt between the samples is 200 μs and n is in the interval $[1, 5]$.

Although the threshold was determined for the system topology shown in Fig. 7.10, it can also be used in case of a change in system conditions. Two cases were studied, i.e., by taking L_{14} and converter 1 out of service, respectively. For these cases, the pre-fault settings for the converter powers are given in Table A.2 in Appendix A.

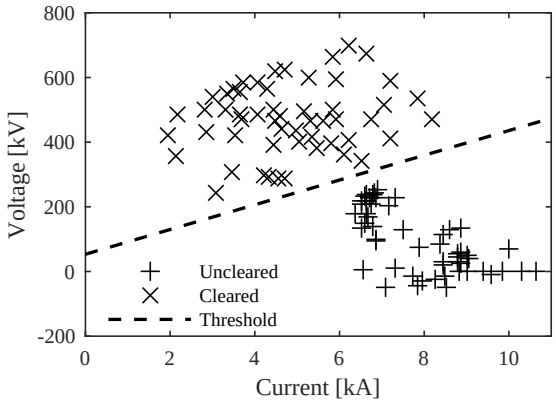


Figure 7.11: Sampled loci of voltage and current measured at R_{13} for nine pole-to-pole faults along L_{13} and threshold for B_{13} breaker failure detection.

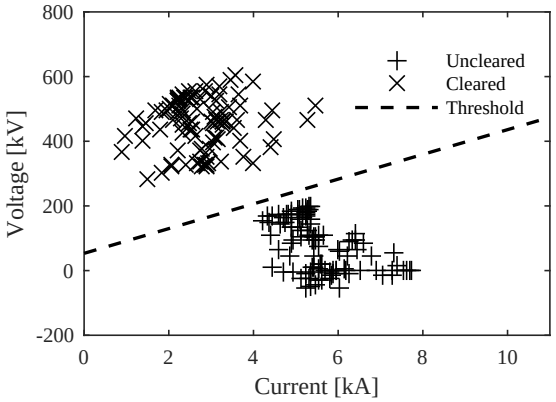


Figure 7.12: Sampled loci of voltage and current measured at R_{13} for nine pole-to-pole faults along L_{13} and threshold for B_{13} breaker failure detection, L_{14} out of service.

For the cases in which L_{14} or converter 1 are taken out of service, the voltage and current samples for uncleared faults shift to the left compared with the base scenario (Figs. 7.12 and 7.13). Nevertheless, in both cases, the threshold of Fig. 7.11 can be used to distinguish between samples for cleared and uncleared faults.

Fig. 7.14 shows the current and voltages measured at R_{13} for both scenarios as described above. The fault creates a traveling wave which arrives at the two

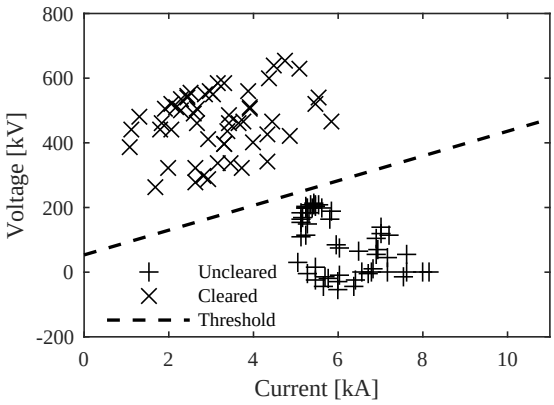


Figure 7.13: Sampled loci of voltage and current measured at R_{13} for nine pole-to-pole faults along L_{13} and threshold for B_{13} breaker failure detection, converter 1 out of service.

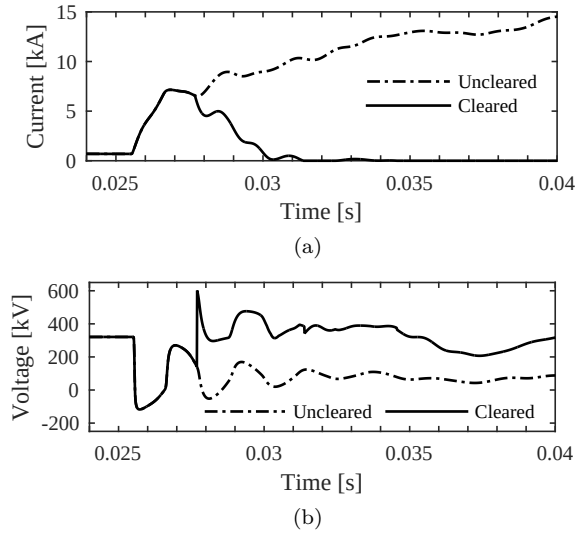


Figure 7.14: Current (a) and voltage (b) measured at R_{13} for a fault in the middle of L_{13}.

terminals of L_{13} at $t = 25.54$ ms due to the finite traveling wave speed. The voltage and current waveforms for the two scenarios differ after $t = 27.65$ ms, which is equal to the sum of the fault inception time and the time required for the wave to travel from the fault location to R_{13}, the fault detection time and

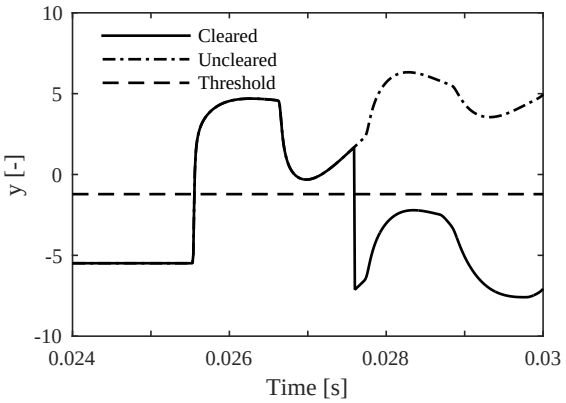


Figure 7.15: Transformed samples y obtained by transformation of the voltage and current measured at R_{13} for a fault in the middle of L_{13}.

breaker opening time. Fig. 7.15 shows the transformed voltage and currents associated with the waveforms for both fault scenarios. After $t = 27.65$ ms, i.e., after primary breaker opening, the projected voltage and current samples associated with the two scenarios can be separated using the threshold y^{thr} (Fig. 7.15).

Classifier

The classifier is trained using a sample set which consists of various fault instances generated by applying faults at the two ends of L_{13} and several points between the two ends (25 km equally-spaced points). For breaker failure detection, the classifier makes use of $k = 1$. To evaluate the classification algorithm, 70% and 30% of the samples are used as training and testing data, respectively.

Fig. 7.16 demonstrates the breaker failure subsystem of R_{13} for the two fault scenarios on L_{13} as described above.

The breaker failure classifier distinguishes cleared from uncleared faults within the time frame of primary protection operation and before the current through the primary breaker becomes zero (Fig. 7.16). Before $t = 25.95$ ms, the class number is 0 which shows that no fault is identified in the primary protection zone. During the interval [25.95, 27.65] ms, the class number is 1 for both scenarios, which indicates that the fault is identified by the primary relay but not yet cleared by the primary breaker. In this stage, the breaker failure subsystem

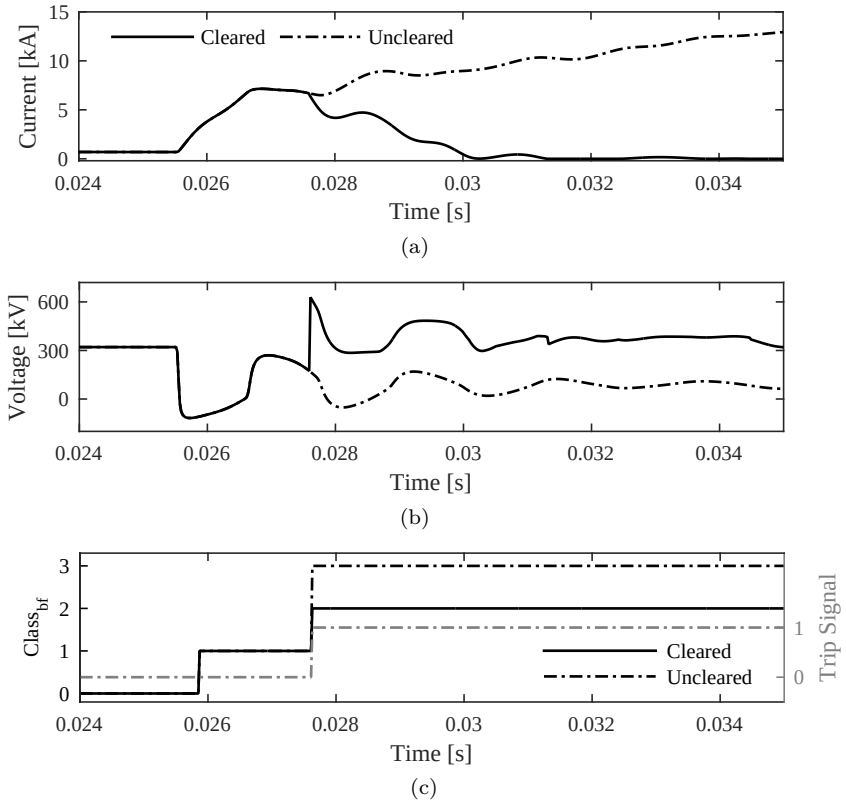


Figure 7.16: Breaker failure detection: positive pole dc current and voltage at R_{13} for scenarios (i) and (ii) (a)-(b), and classifier output (left y-axis) for scenarios (i) and (ii) and breaker failure trip signal for scenario (ii) (right y-axis) (c).

is in the alert state and does not initiate backup actions. At $t = 27.65$ ms, the class number becomes 3 and 2 for scenario (i) and (ii), respectively, indicating that the fault will either be cleared or remains uncleared due to breaker failure.

For scenario (ii), the breaker failure subsystem ensures a fast response by generating a trip signal for the adjacent breakers immediately after B_{13} fails and the classifier output becomes 3 (Fig. 7.16 (b)-(c)). This requires a time delay Δt_{BF} equal to 2 ms, i.e., the breaker opening time. Although the classes are separable directly after $t = 27.65$ ms, a longer delay can be used to increase the protection system's reliability.

7.4.2 Relay Failure Detection

Figs. 7.17-7.19 illustrate the backup protection provided by R_{12} for failure of R_{13} and R_{14} for three scenarios: (i) fault on L_{13} at bus 3 (ii) fault on L_{14} (100 km from bus 1) and (iii) fault on L_{12} at bus 1. Each fault scenario studies two cases where the fault is either detected or not detected by the primary relay. Figs. 7.17-7.19 show the output of the classifier associated with R_{12}.

The sample set of the classifier consists of various fault instances generated by applying faults at the two ends of L_{12}, L_{13} and L_{14} and several points between the two ends (25 km equally-spaced points). For the relay failure subsystem, the classifier for R_{13} makes use of $k = 10$ for pre-classification (fault detection) and $k = 50$ for discrimination between cleared and uncleared faults. Similar to the breaker failure subsystem, 70% and 30% of the samples are used as training and testing data, respectively.

For scenarios (i) and (ii), the relay failure classifier distinguishes cleared from uncleared faults shortly after the instant the primary protection is expected to start fault current interruption (Figs. 7.17 and 7.18 (a) and (b)). In both scenarios, the class number is 0 before fault detection and becomes 2 after the fault is detected in the reverse backup zone. During the time interval in which B_{13} or B_{14} are expected to open, i.e., $[t_{\mathrm{p}}^{\mathrm{d}}\ t_{\mathrm{p}}^{\mathrm{o}}]$, the relay failure subsystem is in the alert state but does not initiate backup actions. Immediately after $t_{\mathrm{p}}^{\mathrm{o}}$, the class number becomes 5 for both uncleared and cleared fault scenarios, indicating that the relay failure subsystem cannot instantly make a correct decision. In less than 0.25 ms from $t_{\mathrm{p}}^{\mathrm{o}}$, the class number for the cleared faults changes to 4, indicating that the primary protection has dealt with the fault. If the class number remains 5, the relay failure subsystem trips all breakers connected to bus 1.

To avoid tripping of all breakers at bus 1 in case the classifier output becomes 5 while the fault is being cleared by B_{13}, Δt_{RF} is set to 3 ms (Figs. 7.17-7.18 (b) and (c)). This time delay provides a margin of 1 ms on top of the primary fault detection and breaker opening time to account for the uncertainty on the classifier output shortly after $t_{\mathrm{p}}^{\mathrm{o}}$.

For scenario (iii), the relay failure classifier correctly distinguishes faults in the primary protection zone from those in the reverse backup protection zone (Fig. 7.19). After fault detection, the output of the classifier becomes 1, stating that the fault is in the primary zone. In 2 ms after fault detection, the classifier output becomes 2 or remains 1, showing that B_{12} has either operated or failed to remove the fault. The relay failure subsystem does not initiate backup actions as it does not enter the alert or action state.

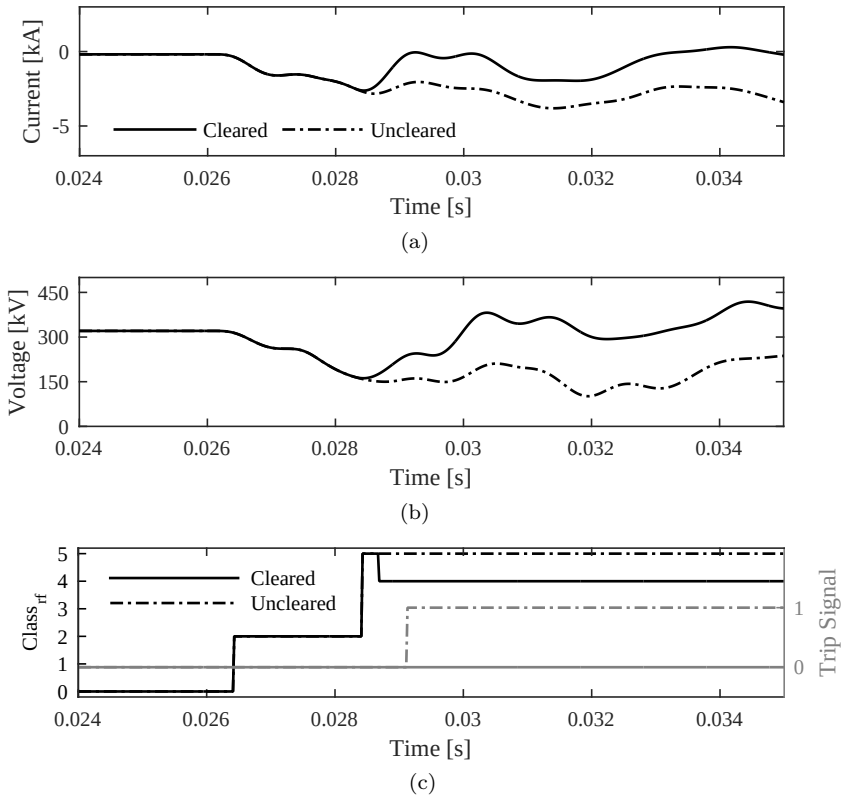


Figure 7.17: Relay failure detection for scenario (i): positive pole dc current and voltage at R_{12} (a)-(b) and classifier output (left y-axis) and relay failure trip signal (right y-axis) (c).

Fig. 7.20 shows that, in this test system, the samples measured at R_{12}, for cleared and uncleared faults at L_{13}, are separable 3 ms after fault detection. Furthermore, with and without the outage of L_{14} or converter 1, the samples associated with faults on L_{13} remain separable. Therefore, the relay failure subsystem remains operable with these changes in system conditions.

7.4.3 Remote Breaker Failure Backup Protection

The remote breaker failure backup protection provided for B_{13} was evaluated using the following scenarios: (i) a pole-to-pole fault at bus 1 cleared by bus 1 primary protection, (ii) a pole-to-pole fault at bus 1 and failure of B_{13} and

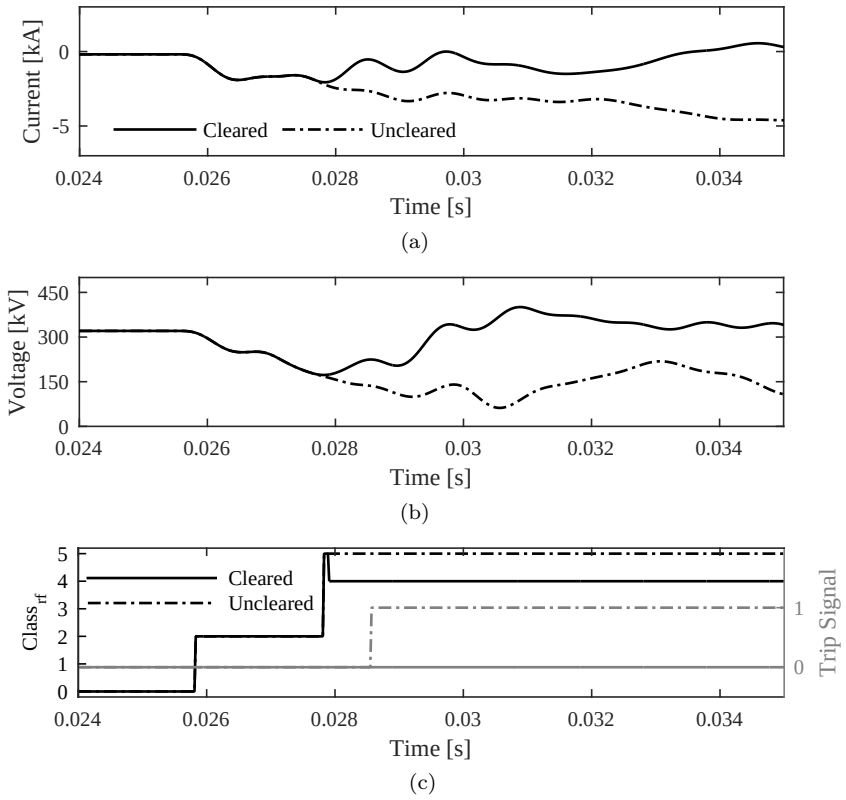


Figure 7.18: Relay failure detection for scenario (ii): positive pole dc current and voltage at R_{12} (a)-(b) and classifier output (left y-axis) and relay failure trip signal (right y-axis) (c).

(iii) pole-to-pole fault at L_{14} cleared by local backup protection (B_{13}, B_{12} and B_{1c} trip 3 ms after fault detection by R_{14}). In scenario (iii), the fault occurs at 0 km from bus 1. The remote backup protection should trip breaker B_{31} for scenario (ii) and not take actions for scenarios (i) and (iii).

To determine the thresholds for the remote breaker failure backup protection at R_{31}, sixteen fault scenarios were simulated and the resulting waveforms at R_{31} were analyzed. Along L_{14} and L_{12}, nine and five fault scenarios were simulated at equally-spaced distances starting at 0 km from bus 1. These faults were cleared by the local breaker failure backup protection provided by B_{14} and B_{12}, respectively. Two fault scenarios with a fault at bus 1 (which were either cleared by the primary protection or remained uncleared due to B_{13} failure) were also

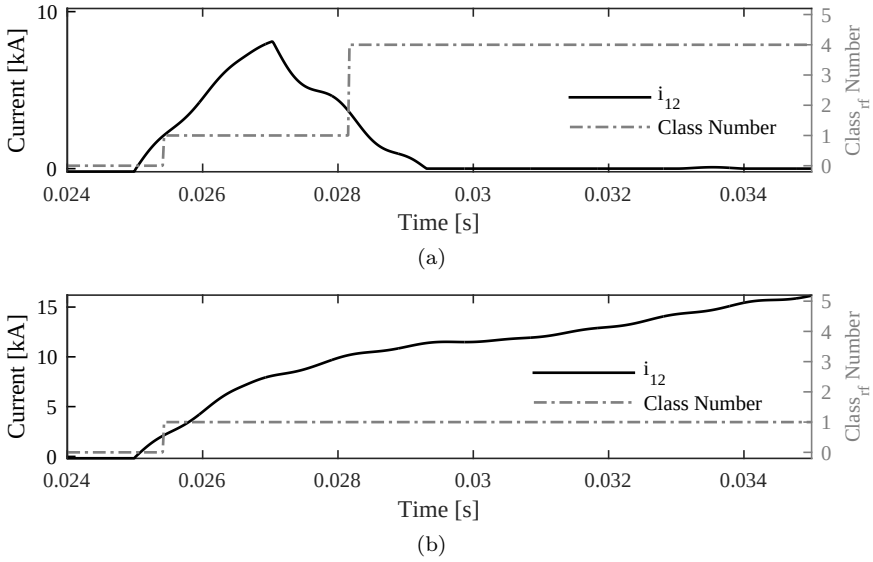


Figure 7.19: Relay failure detection for scenario (iii): dc fault currents at R_{12} (left y-axis) and classifier output (right y-axis) for a detected fault (a) and an undetected fault (b).

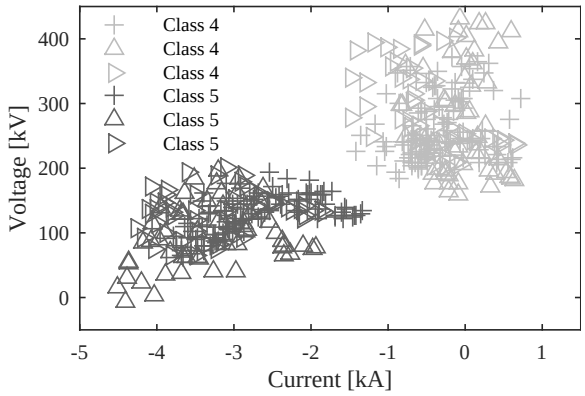


Figure 7.20: Classes associated with 5 equally spaced samples in time interval [$t_{\mathrm{p}}^{\mathrm{d}}$+3 ms,$t_{\mathrm{p}}^{\mathrm{d}}$+4 ms], measured at R_{12} for cleared and uncleared faults on L_{13} (for normal operation (+), with outage of L_{14} ($\triangle$) or outage of converter 1 ($\triangleright$)).

simulated.

The thresholds for the remote backup relay were derived from the waveforms

Table 7.1: Remote backup protection settings.

$u^{\mathrm{thr,d}}$	$u^{\mathrm{thr,id}}$	$i^{\mathrm{thr,id}}$	$u^{\mathrm{thr,uc}}$	Δt^{id}	Δt^{uc}
272 kV	113 kV	1.64 kA	181 kV	1.5 ms	3 ms

of these scenarios and are shown in Table 7.1. $u^{\mathrm{thr,d}}$ was chosen as 85% of the nominal voltage. The time delays were chosen such that $t_{\mathrm{rb}}^{\mathrm{id}}$ and $t_{\mathrm{rb}}^{\mathrm{uc}}$ are 1.5 ms and 3 ms after $t_{\mathrm{p}}^{\mathrm{d}}$, respectively. $u^{\mathrm{thr,id}}$ was set to the minimum voltage measured at R_{31} after line fault detection. $i^{\mathrm{thr,id}}$ was considered to be the maximum current measured at R_{31} at $t_{\mathrm{rb}}^{\mathrm{id}}$. For $u^{\mathrm{thr,uc}}$, the maximum value of the voltage measured at R_{31} for cleared bus faults was taken.

With the thresholds and time delays shown in Table 7.1, the remote backup relay generates a trip signal only for scenario (ii). For all fault scenarios, the backup relay quickly detects the fault, i.e., within 0.2 ms and 0.3 ms after wave arrival at R_{31} for scenarios (i)-(ii) and (iii), respectively (Figs. 7.21-7.22). At $t = 27.8$ ms, the protection algorithm correctly distinguishes the fault at L_{14} from the fault at bus 1. As s_{id} becomes 0 for scenario (iii), the backup protection does not take any action to clear the fault (Fig. 7.22 (c)). For scenarios (i) and (ii), at $t = 29.3$ ms, the backup relay detects a cleared fault and an uncleared bus fault, respectively (Fig. 7.21). Only in scenario (ii), all flag signals become 1 (Fig. 7.21 (c)).

For scenario (ii), the maximum current through B_{31} is reached at $t = 29.3$ ms and becomes zero at $t = 30.6$ ms (Fig. 7.21 (a)). The current through B_{31} again increases after reaching zero. This is due to the simplified model of the dc breaker, as no residual current interrupters are included. The used dc breaker model solely relies on the voltage inserted by the surge arrester to clear the fault.

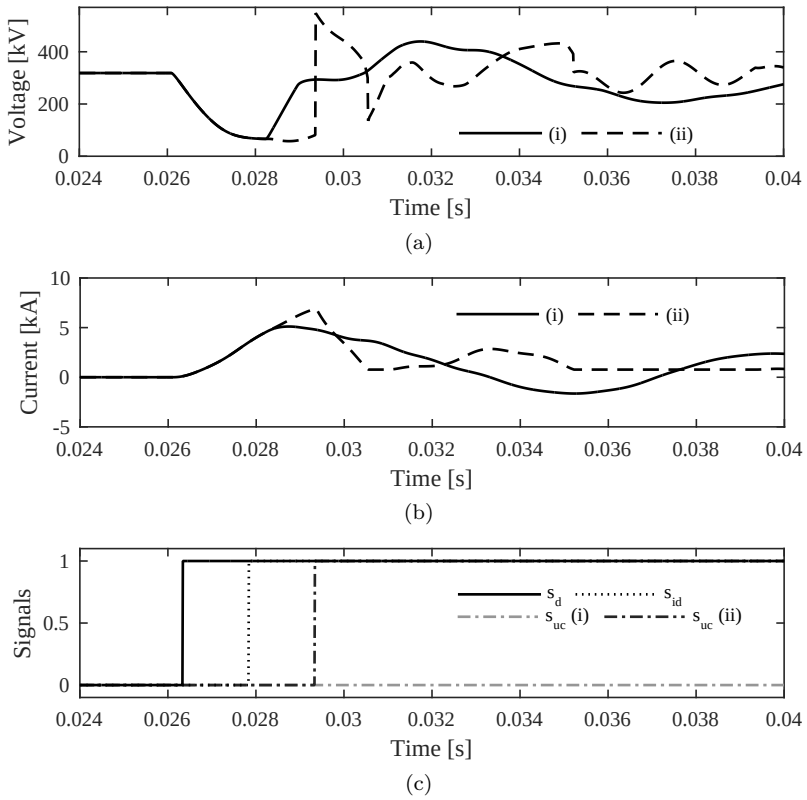


Figure 7.21: Scenarios (i)-(ii): voltage and current measurements at R_{31} (a)-(b) and backup protection signals (c).

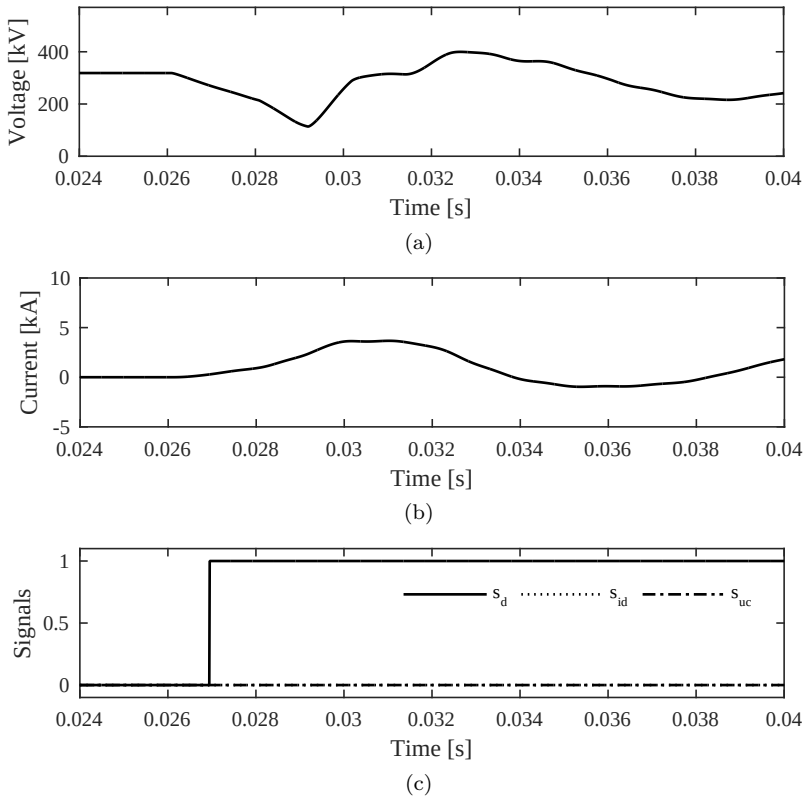


Figure 7.22: Scenario (iii): voltage and current measurements at R_{31} (a)-(b) and backup protection signals (c).

7.5 Conclusion

This chapter proposes two backup protection algorithms for local and remote backup of HVDC grids. The proposed backup protection algorithms result in a fast fault clearance time in case of primary protection failure. The short fault clearance time reduces the exposure of system equipment to low dc voltages and high currents, and therefore, leads to lower required ratings for equipment such as dc breakers and converters. The study results show that the backup protection algorithms detect primary protection failure shortly after the expected breaker opening instant and generate the correct trip signals for their associated breakers.

The principles of the backup algorithms are based on the voltage and current waveforms associated with dc breaker operation for dc breakers employing series inductors. For the local backup protection algorithms, an implementation using a threshold and using a classifier were proposed. The remote backup protection algorithm makes use of thresholds on voltage and current measurements. The determination of the thresholds or the training of the classifiers is done through EMT-simulations of various faults in the grid under study.

The case studies show that the local and remote backup protection algorithms can discriminate uncleared from cleared faults shortly after the breaker opening instant. Furthermore, the case studies demonstrate that the local backup algorithms remain operable also with changes in system conditions such as disconnection of a converter or a line at the bus where the backup relay is located.

Chapter 8

Conclusions and Future Research

This work provides the necessary concepts to develop communication-less protection algorithms for meshed VSC HVDC cable grids through (i) a fundamental analysis of dc fault current phenomena in HVDC grids and (ii) using this analysis to develop protection algorithms applicable for a wide range of meshed HVDC cable grids. First, a detailed overview of dc fault phenomena is provided and fault clearing strategies proposed in the existing literature are discussed and classified. Second, the fault current contribution of the half-bridge MMC is characterized and a reduced converter model for use in dc fault studies is developed. Third, an overview of grounding and configuration options for HVDC grids is provided and their advantages and disadvantages are compared. Fourth, guidelines for the design of fault detection methods in HVDC grids are proposed. These guidelines are based on fundamental traveling wave theory. Furthermore, for the fault detection methods, guidelines for signal processing including the selection of the appropriate sampling frequency and the design of digital filters, are provided. Fifth, selective and fast HVDC grid protection algorithms for primary and backup protection are developed. These algorithms are tailored for a selective fault clearing strategy in meshed VSC HVDC cable grids with inductive cable terminations.

This chapter first gives an overview of the general conclusions of the research conducted in this work, before indicating tracks for future research.

8.1 General Conclusions

8.1.1 Fault Clearing Strategies for HVDC Grids

Fault clearing strategies to deal with dc faults in HVDC grids fundamentally comply to one of two objectives, i.e., to protect the HVDC grid as a system itself or to minimize the impact of the dc fault on the connected ac systems. In the former case, the fault clearing strategy is subject to stringent time constraints in the order of a few to a few tens of milliseconds. In the latter case, the time constraints on fault clearing are less stringent. The fault clearing strategies proposed in the literature can be classified into (i) selective, (ii) alternative, (iii) partially selective and (iv) non-selective, with possible subdivisions in terms of fault clearing equipment or compliance with constraints.

Selective protection of HVDC grids is needed for large scale meshed HVDC grids. Selective protection requires the use of dc circuit breakers and a selective protection algorithm. Partially or non-selective HVDC grid fault clearing strategies put limits to the size or structure of the HVDC grid, as dc sub-grids must be easily definable and the impact on the connected ac systems must be limited.

The time scale of selective fault clearing must be matched to the time scales related to the HVDC grid. Due to the low overcurrent capabilities of power electronic components and tight operating margins on the dc voltage, dc faults must be cleared fast enough to prevent damage to components and collapse of the dc voltage. Consequently, fast protection algorithms are beneficial to reduce requirements on component ratings and to support the stability of the HVDC grid.

8.1.2 Fault Current Analysis

The dc fault current depends on the converter topology used on the one hand and type of fault and system grounding on the other hand. For pole-to-ground faults, the post-fault currents and voltages depend on the type of grounding and grid configuration. Pole-to-pole faults lead to high fault currents and low voltages, irrespective of the type of grounding.

The analysis of the dc fault current contribution of a half-bridge MMC shows that the dc fault current can be divided into contributions due to discharge of the submodule capacitors and infeed by the connected ac system. Before turning off the IGBTs, the submodule capacitors of inserted submodules discharge into the fault. During this stage, the contribution of the ac system to the

dc fault current is limited compared with the capacitive discharge. After the IGBT turn-off instant, the converter enters the blocked state. In this stage, the submodule capacitors no longer contribute to the fault current and the half-bridge MMC becomes an uncontrolled diode rectifier, through which the ac system contributes to the dc fault current.

The grounding type and grid configuration have a direct impact on the HVDC grid design and protection as these determine fault current levels and post-fault voltages after pole-to-ground faults. Furthermore, the grid configuration has an influence on the extensibility of the grid and influences flexibility for post-fault operation. A case study using a three-terminal test system demonstrates that post-fault operating flexibility of a bipolar grid is higher compared with monopolar grids, since the available power transfer capacity can be more effectively used through unbalanced operation.

8.1.3 Modeling for Analysis of Transients Resulting from Dc Faults

Based on the fault current analysis, a reduced converter model for dc fault studies in HVDC grids with half-bridge MMCs was proposed. Furthermore, a four-terminal HVDC grid test system was developed in cooperation with the EE research group at KTH. Until now, only one HVDC grid test system was described in literature. In contrast with this test system, the proposed test system consists of only four dc terminals, which enables implementation in educational versions of commercially available EMT-type software.

The proposed equivalent circuit for half-bridge MMC largely reduces model complexity compared with the models used for benchmarking. It explicitly separates the contribution by the submodule capacitors from that by the ac system. Due to the absence of control loops, its input requirements and model complexity are several times lower than the ones of the models used for benchmarking. Furthermore, since in the equivalent circuit, the capacitive discharge stage is modeled by a passive circuit, the converter can be replaced by an equivalent impedance for dc fault detection and discrimination studies.

8.1.4 Protection Algorithms for Meshed HVDC Grids

Prior to extensive simulations in EMT-type software, fault detection methods for HVDC grids can be designed by identifying the high frequency content of the transient voltages and currents. In the approach proposed in this work, the frequency content of the waveforms at the relay location is obtained

through calculating the transfer function of the voltage and current waves at the relay used for fault detection to the ones at the fault location. The main fault detection signals are voltage and current magnitude and derivative, and detection functions based on a combination of transient voltage and current components. The transfer functions of each signal indicate the presence of high frequency content in the signal, and hence provide an indication for the suitability of the signal in a high speed fault detection method.

The sampling frequency must be sufficiently high to ensure high speed fault detection. The delay introduced by the low-pass filter associated with an analog-to-digital converter increases with decreasing frequency, and results in unacceptable delays for low sampling frequencies. In a case study, the lower limit on the sampling frequency was found to be in the order of 50 kHz if a 10 bit signal representation and associated low-pass filter are used.

To optimally detect dc faults in a noisy environment, matched filter theory can be applied. Application of matched filter theory for dc fault detection leads to filters which implement the first order derivative. A case study in a realistically dimensioned HVDC grid shows that the dc fault detection methods designed using the approach can detect dc faults within hundreds of microseconds. Furthermore, with these methods, dc faults can be discriminated from transients not created by dc faults, e.g., those resulting from faults in the connected ac systems.

The primary protection algorithm proposed in this work makes use of the voltage magnitude and voltage derivative of the first incident wave resulting from a fault to discriminate between faults on the cable and those beyond the series inductor in the forward direction of the relay. To discriminate between faults in the forward and backward direction of the relay, the current derivative is used.

The applicability of the proposed primary protection algorithm for a wide range of grid topologies and parameters is demonstrated by analyzing the impact of the series inductance, cable length, grid topology and fault resistance. A case study using the four-terminal HVDC grid test system shows that the thresholds obtained with the reduced model closely match those obtained with a detailed model in EMT-type software. Furthermore, the case study demonstrates the ability of the proposed protection algorithm to reliably detect and discriminate faults in this system.

The proposed backup protection algorithms result in a fast fault clearance time in case of primary protection failure. The principles of the backup algorithms are based on the voltage and current waveforms associated with fault current interruption by dc breakers. The case studies show that the local and remote backup protection algorithms can discriminate uncleared from cleared

faults shortly after the breaker opening instant. The case studies furthermore demonstrate that the local backup algorithms remain operable also with changes in system conditions such as disconnection of a converter or a line at the bus where the backup relay is located.

8.2 Future Research

As an immediate follow-up, the research in the broad range of topics touched in this work can be continued into a more in-depth analysis towards practical applications. The evaluation of protection algorithms towards practical implementation can benefit from using more detailed measurement models, models for advanced cable systems and detailed converter models, possibly within a real-time environment.

The specification of functional requirements for HVDC grids and the evaluation of fault clearing strategies to comply with these requirements is an essential next step to design the appropriate HVDC grid protection. The functional requirements define the limits within which the system protection is expected to operate. These requirements thus specify the appropriate protection philosophy and its practical implementation in terms of fault clearing equipment, protection algorithms and measurement equipment. The foundations for this analysis were provided in Section 2.2.3 of Chapter 2.

The analysis of protection algorithms for HVDC cable grids provided in this work can be continued for overhead line systems or hybrid cable-overhead line systems. Overhead lines have a higher characteristic impedance and higher traveling wave speed compared with cable systems, which might impact the choice of fault detection method. Furthermore, protection algorithms for such systems must deal with different types of faults and mutual coupling of the poles. The design of protection algorithms for hybrid cable-overhead line systems faces challenges due to reflections of traveling waves at the cable-overhead line interface.

Future work might include integration of the proposed protection algorithms in a communication-based scheme. A communication-based scheme could also be used to coordinate the local and remote backup protection algorithms. For instance, all breaker types currently considered feasible exhibit an inherent time delay before being able to interrupt the fault current. Consequently, the time delay provided by breaker opening can be used to verify the existence of the fault or to verify the occurrence of the fault within the primary protection zone. These time delays might allow the use of communication-based schemes to stop the fault current interruption process. The requirements on the communication

channel, such as maximum acceptable communication delay, required reliability and bandwidth need to be determined.

Finally, the interaction between active grid elements, e.g., converters, breakers or fault current limiters, and the protection algorithms is an interesting track for future research. Converter topologies with different responses to dc faults, e.g., feeding in ac fault currents or having dc fault blocking capability, require a different approach especially when considering backup protection. With fault current limiters or dc breakers, the dc fault current can be altered in various ways. Given the short operation time of primary protection, backup algorithms are likely more affected by the actions of grid elements compared with primary protection algorithms. To allow the design of backup protection algorithms which are generally applicable in a multi-vendor HVDC grid, a standardized response of the grid elements to dc faults must be defined.

Appendix A

HVDC Grid Test System

This appendix describes the layout and component models of the HVDC grid test system developed in cooperation with the EE research group at KTH, and available for download at the link provided in [153]. Additionally, the appendix provides the scenarios describing the pre-fault power flow as used for this work.

For HVDC grids, only one test system has until now been proposed in [154]. In contrast with this test system, the developed test system has a lower complexity and a lower number of terminals. This allows implementation in educational versions of commercially available EMT-type software.

The proposed HVDC grid test system consists of four converters connected by five cables (Fig. A.1). The HVDC grid consists of two links of 200 km length (links 13 and 14), one link of 150 km (link 24) and two links of 100 km (links 12 and 34). Dc breakers are included at the end of each transmission line. The system configuration is symmetric monopolar with a dc pole-to-ground voltage of 320 kV.

A.1 HVDC Grid Components

A.1.1 Ac System

The ac systems are modeled by ac voltage sources in series with an equivalent impedance defining the short circuit power and X/R-ratio. The short circuit power is approximately ten times the rated power of the converter and the X/R-

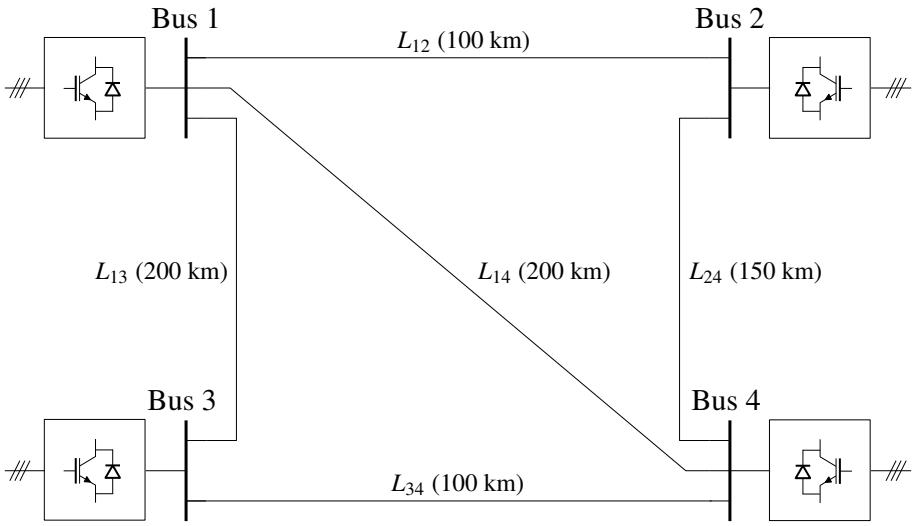


Figure A.1: Four-terminal HVDC grid test system.

Table A.1: Ac system and converter parameters.

	Conv. 1,2,3	Conv. 4	
Rated power	900	1200	[MVA]
Ac grid side voltage	400	400	[kV]
Ac converter side voltage	380	380	[kV]
Transformer leakage reactance	0.15	0.15	[pu]
Ac grid reactance X_{ac}	17.7	13.4	[Ω]
Ac grid resistance R_{ac}	1.77	1.34	[Ω]
Arm capacitance C_{arm}	29.3	39	[μF]
Arm inductor L_{arm}	84.8	63.6	[mH]
Arm resistance R_{arm}	0.885	0.67	[Ω]
Bus filter inductor	10	10	[mH]

ratio is 10. Table A.1 shows the associated values for the ac system reactance X_{ac} and resistance R_{ac}.

A.1.2 Converter

The converters are modeled by the continuous arm model described in Chapter 3 using the parameters shown in Table A.1. The converter is interfaced with the ac system using a transformer with grounded star winding configuration at the ac side and delta winding configuration at the dc side. An inductor of 10 mH is connected in series with the converter and the dc bus. Optionally, a dc side reference can be made using 2.5 μF capacitors at the dc bus.

The higher-level control system of the MMC consists of two outer controllers and separate current controllers for positive and negative sequence current control. The outer controllers are set to control the active and reactive power and provide current references in the *dq*-reference frame to the positive sequence inner controller. For dc voltage control, droop control is added to the active power control loop of converters 3 and 4. The negative sequence current controller suppresses second order harmonics in the dc-side current and voltage during unbalanced ac grid conditions and keeps the ac-side current balanced during asymmetrical fault conditions [155]. The current references for the negative sequence inner controller are set to zero.

The inner control of the MMC is based on the open-loop approach using estimation of stored energies, as described in [156]. Circulating current suppression is provided with a proportional controller using a gain of $R_{\mathrm{a}} = 16$ [157].

The converter internal protection makes use of an undervoltage threshold on the voltage at the converter's dc terminals and an overcurrent threshold on the converter arm currents. The arm overcurrent threshold is based on the current limit imposed by the SOA of the IGBTs. This limit of the IGBTs I_{CM} was determined by taking the maximum value of the arm current for a modulation index of 1. This resulted in a value for I_{CM} of 2.86 kA for converters 1,2 and 3 and 3.86 kA for converter 4. The converter IGBTs are turned off and the converter enters the blocked state if the current through the arm exceeds 0.8 I_{CM}.

A.1.3 Cables

For the links, 320 kV XLPE insulated cables suitable for offshore applications were modeled using the frequency dependent (phase) model available in PSCAD. These cables are described as "Cable 2" in Chapter 3.

A.1.4 Dc Breaker

The dc breaker model represents the basic functionality of a dc breaker, unbound to a specific implementation. Basically, a dc breaker inserts a countervoltage which drives the fault current to zero and absorbs the energy that is present in the system after a fault. The countervoltage is inserted after a certain time delay, depending on breaker technology. The energy absorption is typically performed by a parallel surge arrester, which also determines the maximum countervoltage. Due to the time delay and the high rate of rise of the dc fault current, a series inductor is typically provided to limit the rate of rise of the current [56].

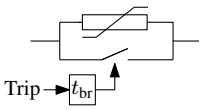


Figure A.2: Dc breaker model.

To incorporate these functions, the breaker is modeled as a switch in parallel with a surge arrester (Fig. A.2). The surge arrester is rated at 150% of the nominal pole-to-ground voltage, i.e., 480 kV. The time delay t_{br} represents the time required by the dc breaker to open after receiving the trip signal.

A.2 Pre-fault Power Flow

Table A.2 shows the converter's active and reactive powers for different scenarios as used in this work.

Table A.2: Pre-fault power flow for each grid topology.

	Base Case		L_{14} out		Conv. 1 out	
	P [MW]	Q [MVar]	P [MW]	Q [MVar]	P [MW]	Q [MVar]
Conv. 1	700 (Rec)	100	700 (Rec)	100	0	100
Conv. 2	700 (Rec)	100	700 (Rec)	100	700 (Rec)	100
Conv. 3	600 (Inv)	100	600 (Inv)	100	300 (Inv)	100
Conv. 4	800 (Inv)	100	800 (Inv)	100	400 (Inv)	100

Appendix B

Detection Function

This appendix elaborates upon the use of traveling wave detection functions for a lossless and lossy line. Additional simulation results for the use of these functions in the case study described in Section 5.4 of Chapter 5 are provided.

B.1 Lossless Line

For a lossless line, the detection function given by:

$$S_1 = u'(t) - R_c i'(t), \tag{B.1}$$

where R_c is equal to Z'_c, can be used to extract backward traveling waves. The solution of the transmission line equations for a lossless line can be written as [106]:

$$u'(t,x) = f_1(t - x/v) + f_2(t + x/v), \tag{B.2}$$

$$i'(t,x) = 1/Z'_c \left(f_1(t - x/v) - f_2(t + x/v)\right), \tag{B.3}$$

in which f_1 and f_2 are functions which represent the forward and backward traveling waves, respectively. Filling in (B.2) and (B.3) in (B.1), and assuming a perfect approximation of Z'_c by R_c, gives $S_1 = 2f_2(t + x/v)$.

For a lossless line, S_1 takes a value of zero for backward faults and $2u_f(t)$ for a forward fault, where $u_f(t)$ is the voltage at the fault location. The use of S_1 for fault detection can be illustrated using the example shown in Figs. B.1 and B.2 (based on the example used in [93]). In these figures, a line AB of length l is

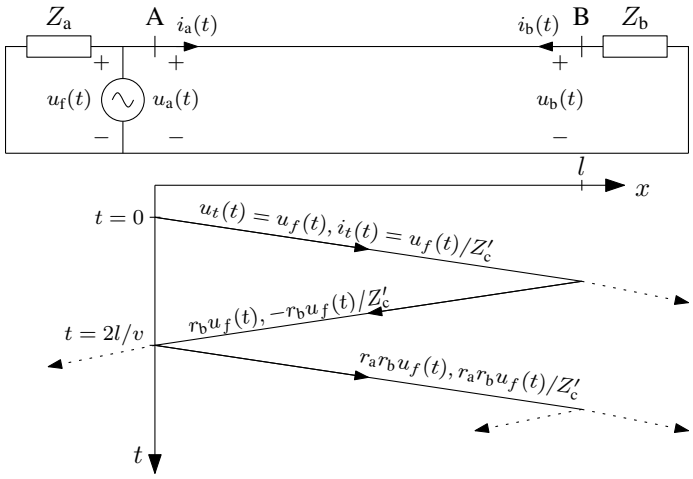


Figure B.1: Lattice diagram for waves traveling on line AB after a fault at $x = 0$ in the backward direction of A.

terminated at both ends by impedances Z_a and Z_b. The voltages and currents are measured at both line ends. In Fig. B.1, a fault occurs at $x = 0$, in the backward direction of A, whereas in Fig. B.2, a fault occurs on line AB at $x = x_\mathrm{f}$. For these cases, f_1 and f_2 can be constructed using a lattice diagram, which shows these functions as a superposition of successively reflected waves as a function of x and t [158]. For a termination impedance consisting only of a real part, the reflection coefficients r_k for $k = \mathrm{a}, \mathrm{b}, \mathrm{f}$ are real and can be calculated as

$$r_k = \frac{Z_k - Z'_\mathrm{c}}{Z_k + Z'_\mathrm{c}}. \tag{B.4}$$

Using $\theta(t)$ to denote the unit step function, $f_1(t, 0)$ and $f_2(t, 0)$ for Fig. B.1 are given by

$$f_1(t, 0) = u_\mathrm{f}(t) \left[1 + r_\mathrm{a} r_\mathrm{b} \theta(t - 2l/v) + ...\right], \tag{B.5}$$

$$f_2(t, 0) = u_\mathrm{f}(t) \left[r_\mathrm{b} \theta(t - 2l/v) + r_\mathrm{a} r_\mathrm{b}^2 \theta(t - 4l/v) + ...\right]. \tag{B.6}$$

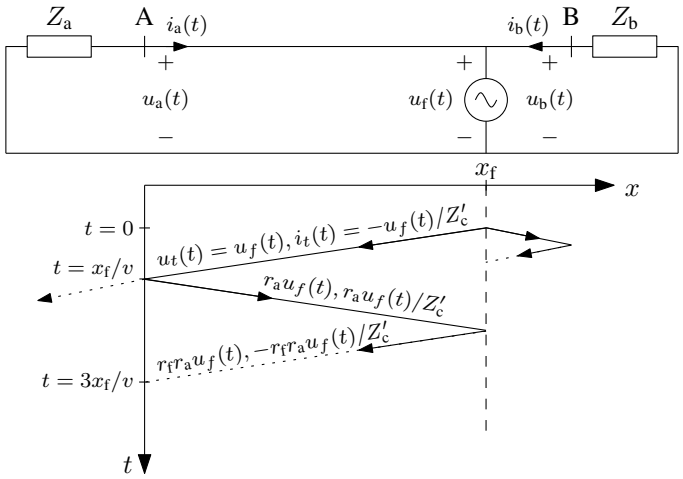


Figure B.2: Lattice diagram for waves traveling on line AB after a fault at $x = x_f$ in the forward direction of A.

Filling in these solutions in (B.2) and (B.3) results in

$$u'(t,0) = u_f(t)\left(1 + (1+r_a)\sum_{m=1}^{\infty} r_a^{m-1} r_b^m \theta(t - m\frac{2l}{v})\right), \tag{B.7}$$

$$i'(t,0) = \frac{u_f(t)}{Z'_c}\left(1 - (1-r_a)\sum_{m=1}^{\infty} r_a^{m-1} r_b^m \theta(t - m\frac{2l}{v})\right). \tag{B.8}$$

Consequently, for a fault in the backward direction of A, $S_1 = 0$ for $0 < t < 2l/v$.

For Fig. B.2, $f_1(t,0)$ and $f_2(t,0)$ are given by:

$$f_1(t,0) = u_f(t)\left[r_a\theta(t - x_f/v) + r_f r_a^2 \theta(t - 3x_f/v) + ...\right], \tag{B.9}$$

$$f_2(t,0) = u_f(t)\left[\theta(t - x_f/v) + r_f r_a \theta(t - 3x_f/v) + ...\right], \tag{B.10}$$

and the associated solutions for $u'(t,0)$ and $i'(t,0)$ are

$$u'(t,0) = u_f(t)(1+r_a)\sum_{m=0}^{\infty}(r_a r_f)^m \theta(t - (2m+1)\frac{x_f}{v}), \tag{B.11}$$

$$i'(t,0) = \frac{-u_f(t)}{Z'_c}(1-r_a)\sum_{m=0}^{\infty}(r_a r_f)^m \theta(t - (2m+1)\frac{x_f}{v}). \tag{B.12}$$

Therefore, for $x_f/v < t < (3x_f)/v$, $S_1 = 2u_f$.

B.2 Lossy Line

For a lossy line, S_1 no longer exactly extracts the backward traveling wave, since $R_\mathrm{c} \neq Z_\mathrm{c}$.

An analysis in the frequency domain demonstrates the use of S_1 for fault detection in case of a lossy line. Taking a similar approach as in Section B.1, the functions F_1 and F_2 can be constructed as a superposition of successively reflected waves. Since $U_\mathrm{a} = F_1 + F_2$ and $I_\mathrm{a} = 1/Z_\mathrm{c}(F_1 - F_2)$, U_a and I_a for a backward fault are given by:

$$U_\mathrm{a} = U_\mathrm{f}\left(1 + (1+\Gamma_\mathrm{a})\sum_{m=1}^{\infty}\Gamma_\mathrm{a}^{m-1}\Gamma_\mathrm{f}^{m}H^{2m}\right), \tag{B.13}$$

$$I_\mathrm{a} = \frac{U_\mathrm{f}}{Z_\mathrm{c}}\left(1 - (1-\Gamma_\mathrm{a})\sum_{m=1}^{\infty}\Gamma_\mathrm{a}^{m-1}\Gamma_\mathrm{f}^{m}H^{2m}\right). \tag{B.14}$$

where $H = e^{-\gamma l}$ and $\Gamma_\mathrm{a,f} = (Z_\mathrm{a,f} - Z_\mathrm{c})/(Z_\mathrm{a,f} + Z_\mathrm{c})$. Filling in these values in (B.1) results in a description of S_1 in the frequency domain:

$$S_1 = (1 - R_\mathrm{c}/Z_\mathrm{c})U_\mathrm{f}. \tag{B.15}$$

In (B.15), $(1 - R_\mathrm{c}/Z_\mathrm{c})$ decreases with increasing frequency. Consequently, for a backward fault, S_1 is not zero, but is equal to U_f passed through the low-pass filter described by $(1 - R_\mathrm{c}/Z_\mathrm{c})$.

For a fault in the forward direction (Fig. B.2), U_a and I_a are given by:

$$U_\mathrm{a} = U_\mathrm{f}(1+\Gamma_\mathrm{a})\sum_{m=0}^{\infty}(\Gamma_\mathrm{a}\Gamma_\mathrm{f})^{m}H^{2m+1}, \tag{B.16}$$

$$I_\mathrm{a} = \frac{-U_\mathrm{f}}{Z_\mathrm{c}}(1-\Gamma_\mathrm{a})\sum_{m=0}^{\infty}(\Gamma_\mathrm{a}\Gamma_\mathrm{f})^{m}H^{2m+1}, \tag{B.17}$$

where $H = e^{-\gamma x_\mathrm{f}}$. Taking the solution for $m = 0$ (i.e., considering the solution valid for the time interval $x_\mathrm{f}/v < t < 3x_\mathrm{f}/v$) and filling in these values in (B.1) results in:

$$S_1 = \left[(1 + R_\mathrm{c}/Z_\mathrm{c} + \Gamma_\mathrm{a}(1 - R_\mathrm{c}/Z_\mathrm{c}))\right] HU_\mathrm{f}. \tag{B.18}$$

As a result, fault detection using S_1 is no longer termination independent and depends on the choice of R_c.

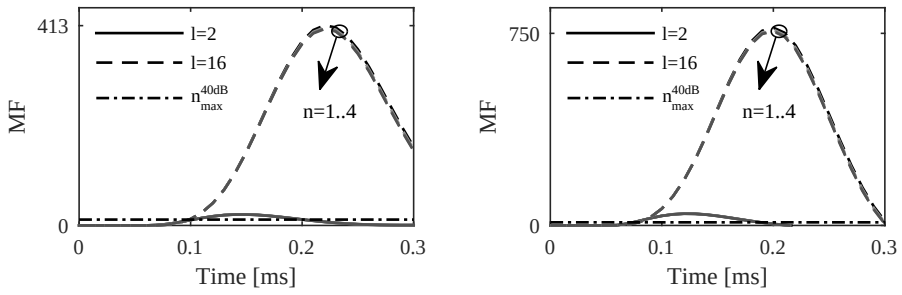


Figure B.3: Time response $S_{1,L4}^{\mathrm{MF},l}$ for matched filters of length 2 and 16 applied to $S_{1,L4}$ for u_{f} given by (5.21) and maximum value for 40 dB white Gaussian noise $n_{\mathrm{max}}^{40\mathrm{dB}}$ for F_3 (a) and F_4 (b), where the number of cables n directly attached to Hub 2 is varied from 1 to 4.

B.3 Case Study

In Section B.3.1, the influence of the termination impedance on fault detection using (5.16) and (5.19) is investigated for the case study described in Chapter 5. In Section B.3.2, the response of (5.16) to faults in the backward direction is evaluated.

B.3.1 Influence of Termination Impedance

To evaluate the influence of the termination impedance, the number of cables directly attached to Hub 2, i.e., $L5 - L8$, is varied from $n = 1$ to $n = 4$ (Fig. 5.4) and $S_{1,\mathrm{L4}}^{\mathrm{MF},2}$ and $S_{1,\mathrm{L4}}^{\mathrm{MF},16}$ are calculated for F_3 and F_4. To calculate $S_{1,\mathrm{L4}}^{\mathrm{MF},2}$ and $S_{1,\mathrm{L4}}^{\mathrm{MF},16}$, the time domain response of (D.11) and (D.12) is first calculated for a step input of U_{f} given by (5.20), resulting in $u_{\mathrm{h},2}(t)$. The current $i_{\mathrm{h},2}(t)$ is found using a similar procedure. Thereafter, an ADC with a third order Butterworth filter associated with a sampling frequency of 100 kHz is used to obtain $u_{\mathrm{h},2}^{\mathrm{LP}}(kT)$ and $i_{\mathrm{L4}}^{\mathrm{LP}}(kT)$.

For F_3 and F_4, the variation of $S_{1,\mathrm{L4}}^{\mathrm{MF},2}$ and $S_{1,\mathrm{L4}}^{\mathrm{MF},16}$ with n is limited (Fig. B.3). The difference between $S_{1,\mathrm{L4}}^{\mathrm{MF},2}$ and $S_{1,\mathrm{L4}}^{\mathrm{MF},2}$ for $n = 1$ and $n = 4$ is calculated as:

$$\epsilon_{\mathrm{abs}}^{2} = S_{1,\mathrm{L4}}^{\mathrm{MF},2}|_{n=1} - S_{1,\mathrm{L4}}^{\mathrm{MF},2}|_{n=4}, \tag{B.19}$$

$$\epsilon_{\mathrm{abs}}^{16} = S_{1,\mathrm{L4}}^{\mathrm{MF},16}|_{n=1} - S_{1,\mathrm{L4}}^{\mathrm{MF},16}|_{n=4}, \tag{B.20}$$

and is shown in Fig. B.4. For both faults and filter lengths, the maximum absolute difference correspond to a relative difference lower than 5%.

B.3.2 Fault Detection Criteria for Backward Faults

The response of S_1 for backward faults is determined by evaluating (B.15) for a step input of -300 kV for $u_{\mathrm{f}}(t)$ and passing the result through matched filters of length 2 and 16 as shown in Fig. 5.10. Fig. B.5 shows the response of the matched filters for S_1 as given by (B.15). For $S_1^{\mathrm{MF},2}$, the filter output does not exceed the noise threshold of 40 dB, whereas $S_1^{\mathrm{MF},16}$ exceeds this threshold at $t = 0.15$ ms. To avoid false detection of backward faults by this criterion, several options are possible:

- Set the threshold to the maximum output of the filters for backward faults. In this case, the detection threshold for the filter of length 16 would be 35 instead of 11.78. This leads to a longer detection time and a less sensitive algorithm,
- Use the current derivative to determine the direction of the fault, where a negative value indicates a fault in the backward direction, or
- Use local communication between relays attached to the same bus. For line faults, one of the relays detects a fault in the forward direction and can use this information to “lock” the other relays.

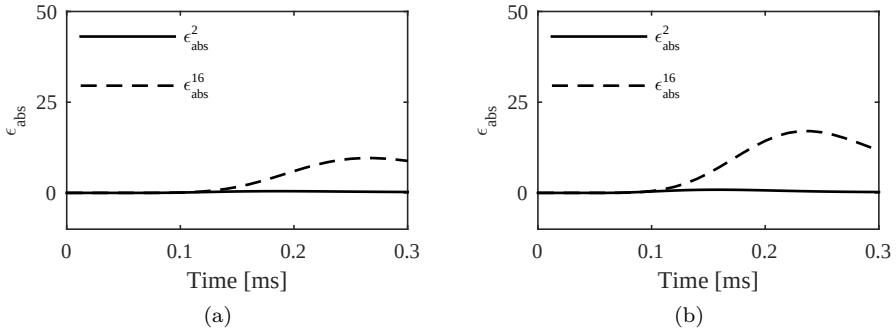


Figure B.4: Absolute differences ϵ^2_{abs} and $\epsilon^{16}_{\text{abs}}$ for F_3 (a) and F_4 (b).

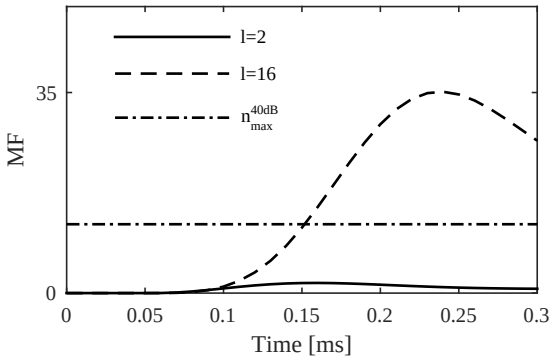


Figure B.5: Time response for matched filters of length 2 and 16 applied to S_1 given by (B.15) for a step input in U_{f} of -300 kV.

Appendix C

Analog Filter Design

In this appendix, the analog filter design for use in the measurement electronics model introduced in Section 5.3.2 of Chapter 5 is explained in detail.

An analog-to-digital converter (ADC) is characterized by the number of bits B, specifying the dynamic range of the device, and the sampling frequency $f_\mathrm{s} = t/T$, specifying the bandwidth of the device. A general scheme for an ADC is given in Fig. C.1. The scheme includes (i) an analog pre-filter to prevent aliasing of noise with frequency components above $f_\mathrm{s}/2$, (ii) a sampler and quantizer to discretize the signal in time and amplitude, respectively, and (iii) a digital filter to post-process the discretized signal. The output of the ADC is $x_\mathrm{Q}(kT)$, which corresponds to a signal $x(t)$ quantized with words consisting of B bits and sampled at time steps kT. Depending on the type of ADC, only an analog or both analog and digital filters are used. In this work, only an analog pre-filter is considered.

An ideal analog pre-filter suppresses the noise above $f_\mathrm{s}/2$ to values below the SNR of the ADC. The SNR or the signal to quantization noise of an ideal ADC depends on the number of bits and is approximately given by $SNR = 6B$ dB, i.e., the SNR increases with 6 dB per bit [159]. Consequently, the analog pre-filter ideally attenuates components above $f_\mathrm{s}/2$ by at least $6B$ dB*.

The analog pre-filter is a low-pass filter characterized by four main parameters: cut-off frequency f_c, stop-band frequency f_stop, pass-band gain A_pass and stop-

*A more elaborate formula can be obtained through stochastic analysis of the input signal and quantization noise and results in $SNR = 6.02B + 16.81 - 20\log(R/\sigma_x)$, in which R is the range of the ADC and σ_x is the variance of the input signal x. For instance, considering a Gaussian distribution for x and taking $R = 6\sigma_x$, $SNR = 6.02B + 1.25$ dB [160].

band gain A_{stop} (Fig. C.2). For an ideal low-pass filter, the pass-band ripple ϵ_{pass} is zero and $f_{\text{c}} = f_{\text{stop}}$. The practical implementations of a low-pass filter, e.g., Butterworth, Chebyshev or Bessel filters, differ in (i) pass-band ripple, (ii) frequency roll-off around f_{c} and (iii) linearity of the phase response (resulting in distortion of the waveform in the time domain response). Table C.1 qualitatively compares these characteristics.

In this work, a Butterworth filter is chosen since it provides a trade-off between the frequency roll-off and time response. In case the shape of the waveform is of primary interest, a Bessel filter should be used. The magnitude response of an n-th order Butterworth filter is given by

$$|H(j\omega)|^2 = \frac{1}{1 + (\omega/\omega_{\text{c}})^{2n}}, \tag{C.1}$$

in which ω_{c} is the cut-off frequency in rad/s. Above f_{c}, the attenuation increases with $20n$ dB/decade.

To design an n-th order Butterworth filter given a certain number of bits B and sampling frequency f_{s}, A_{pass} and A_{stop} are taken as 0 and $6B$ dB, respectively and f_{stop} is set to $f_{\text{s}}/2$. Consequently, f_{c} for an n-th order Butterworth filter can be found as:

$$f_{\text{c}} = \frac{f_{\text{s}}}{2} 10^{-\frac{20n}{6B}}. \tag{C.2}$$

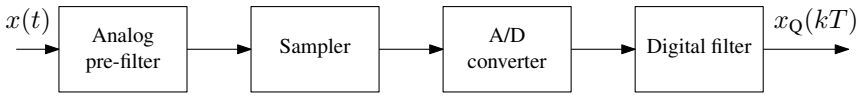


Figure C.1: General analog-to-digital converter scheme.

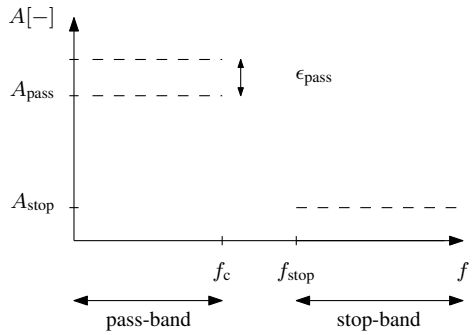


Figure C.2: Main parameters for low-pass filter design.

Table C.1: Comparison of low-pass filters.

	Chebyshev	Butterworth	Bessel
Pass-band ripple	Present	None	None
Frequency roll-off	Highest	Average	Lowest
Transient response	Poorest	Average	Best

Appendix D

Fault Transfer Function

This appendix first explains the construction of the transfer functions of the voltage and current waves at the relay used for fault detection to the ones at the fault location. Second, the transfer functions for the faults in the case study described in Section 5.4 of Chapter 5 are provided.

D.1 Construction Procedure

The construction of transfer functions of the voltage and current at the fault location is illustrated using the circuit shown in Fig. D.1. In this circuit, a cable is terminated by a termination impedance Z_{t} and a fault occurs behind an impedance Z_{f} at a location x_{f} from a relay R located at the cable termination. The pre-fault voltage is U^0. At the fault location, following equations apply for U_{f}:

$$U_{\mathrm{f}} = U'_{\mathrm{f}} + I_{\mathrm{f}} Z_{\mathrm{f}}, \tag{D.1}$$

$$U_{\mathrm{f}} = B_j - I_{\mathrm{f}} Z_{\mathrm{c}}, \tag{D.2}$$

where U'_{f} describes the change in voltage at the fault location compared with the pre-fault voltage. For the first incident wave, $B_j = 0$, and

$$U_{\mathrm{f}} = \frac{Z_{\mathrm{c}}}{Z_{\mathrm{f}} + Z_{\mathrm{c}}} U'_{\mathrm{f}}. \tag{D.3}$$

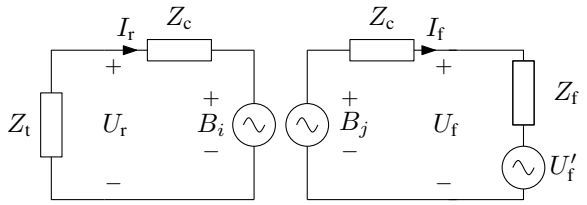


Figure D.1: Cable with termination impedance Z_t and fault behind impedance Z_f.

Using (D.3) and $I_\mathrm{f} = -U_\mathrm{f}/Z_\mathrm{c}$, the forward traveling wave at the fault location can be described as:

$$F_j = 2\frac{Z_\mathrm{c}}{Z_\mathrm{f} + Z_\mathrm{c}} U'_\mathrm{f}. \tag{D.4}$$

At the relay location, following equations apply for U_r:

$$U_\mathrm{r} = Z_\mathrm{t} I_\mathrm{r}, \tag{D.5}$$

$$U_\mathrm{r} = B_i + Z_\mathrm{c} I_\mathrm{r}. \tag{D.6}$$

Using $B_i = HF_j$, where $H = e^{-\gamma x_\mathrm{f}}$ and eliminating I_r, U_r can be found as:

$$U_\mathrm{r} = \frac{2Z_\mathrm{t}}{Z_\mathrm{c} + Z_\mathrm{t}} H \frac{Z_\mathrm{c}}{Z_\mathrm{c} + Z_\mathrm{f}} U'_\mathrm{f}. \tag{D.7}$$

Using (5.5) for Γ, (D.7) can be seen as in the form:

$$U_\mathrm{r} = (1 + \Gamma) H U_\mathrm{f}. \tag{D.8}$$

D.2 Fault Transfer Functions for F_1 to F_4

Using the approach of Section D.1, the transfer functions from the voltage at the fault location to the relays can be constructed for F_1 to F_4. For F_1, the transfer function is given by:

$$\frac{U_2}{U_\mathrm{f}} = H_\mathrm{L3} H_\mathrm{L2} \left(\frac{2Z_\mathrm{A}^\mathrm{conv}}{3Z_\mathrm{A}^\mathrm{conv} + Z_\mathrm{c}} \right) \left(2\frac{Z^\mathrm{Ls} Z_\mathrm{c} + 5Z^\mathrm{Ls} Z_\mathrm{E}^\mathrm{conv} + Z_\mathrm{c} Z_\mathrm{E}^\mathrm{conv}}{Z^\mathrm{Ls} Z_\mathrm{c} + 5Z^\mathrm{Ls} Z_\mathrm{E}^\mathrm{conv} + 6Z_\mathrm{c} Z_\mathrm{E}^\mathrm{conv} + (Z_\mathrm{c})^2} \right), \tag{D.9}$$

in which $H_\mathrm{L3} = e^{-256 \cdot 10^3 \gamma}$, $H_\mathrm{L2} = e^{-101 \cdot 10^3 \gamma}$, $Z^\mathrm{Ls} = sL_2^\mathrm{s}$ and $Z_\mathrm{A}^\mathrm{conv}$ and $Z_\mathrm{E}^\mathrm{conv}$ are the converter impedance of the converters at OWF A and E, respectively. For F_2, the transfer function is given by:

$$\frac{U_2}{U_\mathrm{f}} = H_\mathrm{F2} \left(2\frac{Z^\mathrm{Ls} Z_\mathrm{c} + 5Z^\mathrm{Ls} Z_\mathrm{E}^\mathrm{conv} + Z_\mathrm{c} Z_\mathrm{E}^\mathrm{conv}}{Z^\mathrm{Ls} Z_\mathrm{c} + 5Z^\mathrm{Ls} Z_\mathrm{E}^\mathrm{conv} + 6Z_\mathrm{c} Z_\mathrm{E}^\mathrm{conv} + (Z_\mathrm{c})^2} \right), \tag{D.10}$$

where $H_{\mathrm{F2}} = e^{-25 \cdot 10^3 \gamma}$.

In (D.9), the first and second term between brackets are the refraction coefficients at Hub 1 and 2, respectively. Taking $Z^{\mathrm{conv}} >> Z_{\mathrm{c}}$ and $Z^{\mathrm{Ls}} >> Z_{\mathrm{c}}$ for $\omega \to \infty$, these terms can be reduced to 2/3 and 2, respectively. These values correspond to a termination consisting purely of the cables of L1 and L2 at Hub 1 and an open circuit at Hub 2.

For F_3 and F_4, the transfer function is given by:

$$\frac{U_{\mathrm{h,2}}}{U_{\mathrm{f}}} = H_{\mathrm{L4}} \frac{2Z_{\mathrm{E}}^{\mathrm{conv}}(Z^{\mathrm{Ls}} + Z_{\mathrm{c}})}{(1+n)Z_{\mathrm{E}}^{\mathrm{conv}} Z^{\mathrm{Ls}} + (2+n)Z_{\mathrm{E}}^{\mathrm{conv}} Z_{\mathrm{c}} + Z^{\mathrm{Ls}} Z_{\mathrm{c}} + (Z_{\mathrm{c}})^2}, \qquad \text{(D.11)}$$

$$\frac{U_{\mathrm{h,2}}}{U_{\mathrm{f}}} = H_{\mathrm{F4}} \frac{2Z_{\mathrm{E}}^{\mathrm{conv}}(Z^{\mathrm{Ls}} + Z_{\mathrm{c}})}{(1+n)Z_{\mathrm{E}}^{\mathrm{conv}} Z^{\mathrm{Ls}} + (2+n)Z_{\mathrm{E}}^{\mathrm{conv}} Z_{\mathrm{c}} + Z^{\mathrm{Ls}} Z_{\mathrm{c}} + (Z_{\mathrm{c}})^2}, \qquad \text{(D.12)}$$

where $H_{\mathrm{L4}} = e^{-174 \cdot 10^3 \gamma}$ and $H_{\mathrm{F4}} = e^{-25 \cdot 10^3 \gamma}$ and n is the number of cables (except for the faulted cable) directly attached to Hub 2. For $\omega \to \infty$ and $n = 4$, the fraction term reduces to 2/5, which corresponds to a termination consisting of the four cables of links L5-L8 attached to Hub 2.

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List of Publications

Reviewed Journals

Published

1. S. Pirooz Azad, W. Leterme and D. Van Hertem, "Fast breaker failure backup protection for HVDC grids," in Electric Power Systems Research Special Issue: Papers from the 11th International Conference on Power Systems Transients (IPST), vol. 138, pp. 99-105, Jun. 2016
2. W. Leterme, S. Pirooz Azad and D. Van Hertem, "A local backup protection algorithm for HVDC grids," in IEEE Trans. Power Del., vol. 31, no. 4, pp. 1767-1755, Aug. 2016
3. W. Leterme, J. Beerten and D. Van Hertem, "Nonunit protection of HVDC grids with inductive dc cable termination," in IEEE Trans. Power Del., vol. 31, no. 2, pp. 820-828, Apr. 2016
4. W. Leterme, P. Tielens, S. De Boeck and D. Van Hertem, "Overview of grounding and configuration options for meshed HVDC grids," in IEEE Trans. Power Del., vol. 29, no. 6, pp. 2467-2475, Dec. 2014
5. W. Leterme, F. Ruelens, B. Claessens and R. Belmans, "A flexible stochastic optimization method for wind power balancing with PHEVs," in IEEE Trans. Smart Grid, vol. 5, no. 3, pp. 1238-1245, May 2014

Under Review

6. W. Leterme, M. Barnes and D. Van Hertem, "Fundamental basis and signal processing for traveling wave based fault detection in HVDC grids," submitted to CSEE Journal of Power and Energy Systems, 2016

Book Contributions

7. W. Leterme and D. Van Hertem, "Dc fault phenomena and dc grid protection", in *HVDC Grids for Offshore and Supergrid of the Future*, D. Van Hertem, O. Gomis-Bellmunt and J. Liang (eds.), Hoboken, NJ: J. Wiley & Sons, 2016, ch. 17
8. CIGRÉ Working Group B4/B5-59, "Local control and protection of HVDC grids", [to be published]

International Conferences

9. W. Leterme, J. Beerten and D. Van Hertem, "Equivalent circuit for half-bridge MMC dc fault current contribution", in Proc. IEEE ENERGYCON 2016, Leuven, Belgium, 4-8 Apr. 2016, 6 pages
10. W. Leterme, S. Pirooz Azad and D. Van Hertem, "Fast breaker failure backup protection for HVDC grids", in Proc. IPST 2015, Cavtat, Croatia, 15-18 Jun. 2015, 6 pages
11. W. Leterme and D. Van Hertem, "Classification of fault clearing strategies for HVDC grids", in Proc. CIGRÉ Lund, Lund, Sweden, 27-28 May 2015, 10 pages (art.nr. 143)
12. B. Geebelen, W. Leterme and D. Van Hertem, "Analysis of dc breaker requirements for different HVDC grid protection schemes", in Proc. IET ACDC 2015, Birmingham, UK, 10-12 Feb. 2015, 7 pages
13. W. Leterme, N. Ahmed, J. Beerten, L. Ängquist, D. Van Hertem and S. Norrga, "A new HVDC grid test system for HVDC grid dynamics and protection studies in EMT-type software",in Proc. IET ACDC 2015, Birmingham, UK, 10-12 Feb. 2015, 7 pages
14. S. Pirooz Azad, W. Leterme and D. Van Hertem, "A dc grid primary protection algorithm based on current measurements", in proc. EPE'15 ECCE-Europe, Geneva, Switzerland, 8-10 Sep. 2015, 10 pages
15. J. Tant, W. Leterme, J. Beerten, W. Michiels and J. Driesen, "Generic circuit partitioning method for efficient simulation of modular multilevel converter topologies", in Proc. COMPEL 2014, Santander, Spain, 22-25 Jun. 2014, 8 pages
16. W. Leterme and D. Van Hertem, "Reduced modular multilevel converter model to evaluate fault transients in dc grids", in Proc. IET DPSP 2014, Copenhagen, Denmark, 31 Mar. - 3 Apr. 2014, 6 pages

17. S. Breugelmans, W. Leterme, D. Van Hertem and R. Marcelis, "Comparison of different methods to limit short circuit currents in dc traction networks", in Proc. IET DPSP 2014, Copenhagen, Denmark, 31 Mar. - 3 Apr. 2014, 6 pages

18. F. Ruelens, S. Weckx, W. Leterme, S. Vandael, B. Claessens, and R. Belmans, "Stochastic portfolio management of an electric vehicles aggregator", in Proc. ISGT 2013, Copenhagen, 6-9 Oct. 2013, 5 pages

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